



MMIC DIE

# Power Amplifier

## PMA5-83-2W-D+

50Ω 0.01 to 10 GHz 2 W P<sub>SAT</sub>

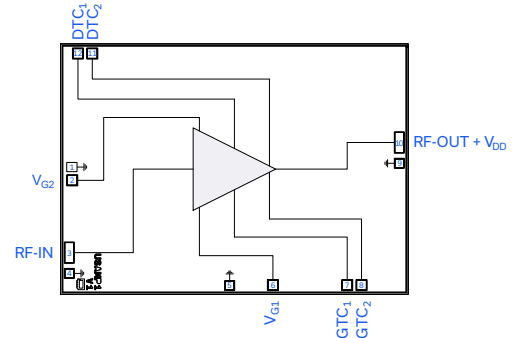
### THE BIG DEAL

- P<sub>1dB</sub>, Typ. +31 dBm
- P<sub>SAT</sub>, Typ. +33 dBm
- Low Noise Figure, Typ. 3.5 dB
- High OIP<sub>3</sub>, Typ. +43.5 dBm
- Supply Voltage +12 V, 400 mA

### APPLICATIONS

- Test and Measurement Equipment
- Radar, EW, and ECM Defense Systems
- 5G Sub6, MIMO Wireless Infrastructure Systems
- Microwave Radio & VSAT

### FUNCTIONAL DIAGRAM



SEE ORDERING INFORMATION ON THE LAST PAGE

### PRODUCT OVERVIEW

The PMA5-83-2W-D+ is a GaAs MMIC Distributed Power Amplifier operating from 0.01 to 10 GHz. The amplifier provides 12 dB of gain, +33 dBm saturated output power, and achieves +43.5 dBm output IP<sub>3</sub>, while operating from a +12 V power supply and consuming 400 mA of current. In addition, the die is internally matched to 50 Ohms. These characteristics make it ideally suited for wideband test instrumentation and defense systems that require high operating output power, while maintaining very low distortion characteristics.

### KEY FEATURES

Features	Advantages
High P <sub>1dB</sub> Typ. +31 dBm	Flat gain and output power make this device excellent for wideband systems from 0.01 to 10 GHz that require at least 1 W of operating power over the full band.
High OIP <sub>3</sub> Typ. +43.5 dBm	High operating OIP <sub>3</sub> and low 2nd and 3rd harmonic response provides for very low in-band distortion products, which is typically needed for high fidelity measurement systems.
Low Noise Figure Typ. 3.5 dB	High operating output power accompanied with low noise figure enables a significant signal to noise ratio advantage for systems requiring high dynamic range.
Unpackaged Die	Suitable for chip and wire hybrid assemblies.



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Mini-Circuits

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### ELECTRICAL SPECIFICATIONS<sup>1</sup> AT +25°C, V<sub>DD</sub> = +12 V, UNLESS NOTED OTHERWISE

Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Frequency Range		0.05		10	GHz
Gain	0.05		18.0		dB
	2		13.2		
	4		13.1		
	6		13.0		
	8		12.6		
	10		12.0		
Output Power at 1 dB Compression (P1dB)	0.5		+29.6		dBm
	2		+31.0		
	4		+31.6		
	6		+31.3		
	8		+30.9		
	10		+30.7		
Output Power at 3 dB Compression (P3dB)	0.5		+30.9		dBm
	2		+32.5		
	4		+33.3		
	6		+33.3		
	8		+33.3		
	10		+32.8		
Output Power at Saturation (P <sub>SAT</sub> ) <sup>2</sup>	0.5		+31.9		dBm
	2		+33.1		
	4		+33.7		
	6		+33.6		
	8		+33.5		
	10		+32.9		
Output Third-Order Intercept (P <sub>OUT</sub> = +20 dBm/Tone)	1		+46.0		dBm
	2		+44.5		
	4		+43.9		
	6		+42.1		
	8		+40.4		
	10		+37.8		
Input Return Loss	0.05		20		dB
	2		12		
	4		20		
	6		20		
	8		15		
	10		17		
Output Return Loss	0.05		11		dB
	2		14		
	4		12		
	6		14		
	8		14		
	10		15		





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### ELECTRICAL SPECIFICATIONS<sup>1</sup> AT +25°C, V<sub>DD</sub> = +12 V, UNLESS NOTED OTHERWISE (CONTINUED)

Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Isolation	0.05		73		dB
	2		48		
	4		41		
	6		38		
	8		35		
	10		33		
Noise Figure <sup>3</sup>	0.5		6.8		dB
	2		3.7		
	4		2.8		
	6		2.9		
	8		3.3		
	10		4.1		
Device Operating Voltage (V <sub>DD</sub> )			+12	+16	V
Device Operating Current (I <sub>DD</sub> ) <sup>4</sup>			400		mA
Gate Voltage (V <sub>G1</sub> )			-0.8		V
Gate Current (I <sub>G1</sub> )			15	4,000	μA
Gate Voltage (V <sub>G2</sub> )			+5		V
Gate Current (I <sub>G2</sub> )			15	4,000	μA
DC Current Variation vs. Temperature <sup>5</sup>			11		μA/°C

1. Tested on Mini-Circuits Die Characterization Test Board. See Figure 2. De-embedded to the device reference plane.

2. P<sub>SAT</sub> defined as when the Output Power changes 0.1 dB per 1 dB change in Input Power.

3. Noise Figure performance taken from packaged version of amplifier, PMA5-83-2W+.

4. Current at P<sub>IN</sub> = -25 dBm. Increases to 650 mA at P1dB.

5. (Current at +85°C - Current at -45°C)/(130°C). VGS held constant over temperature.



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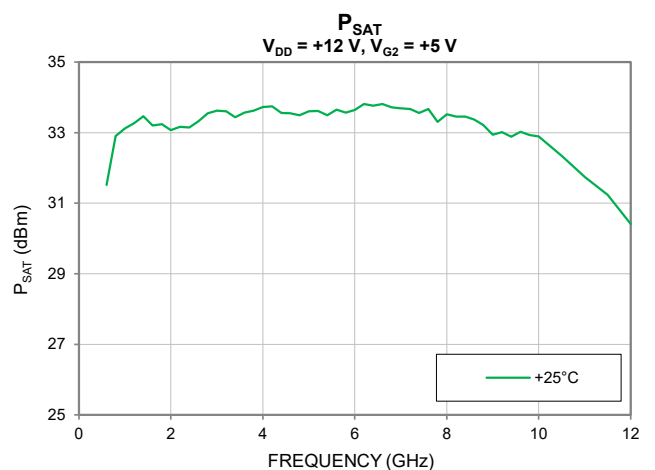
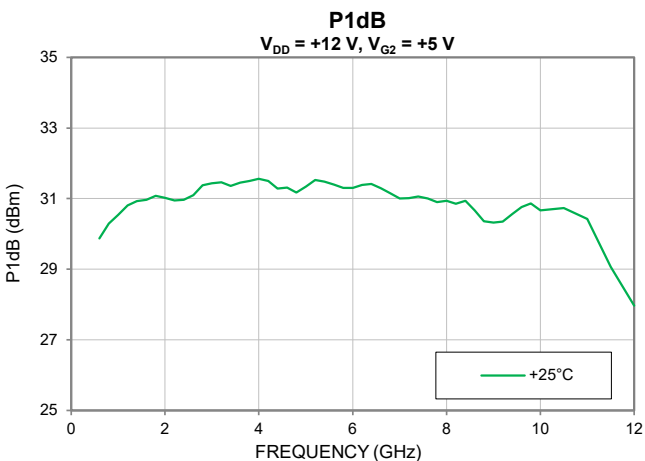
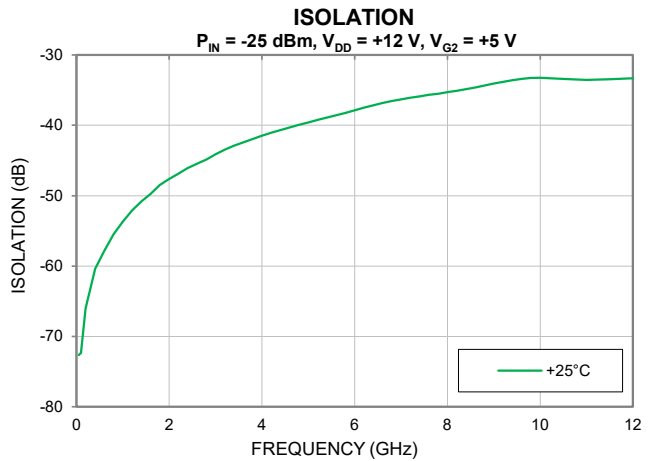
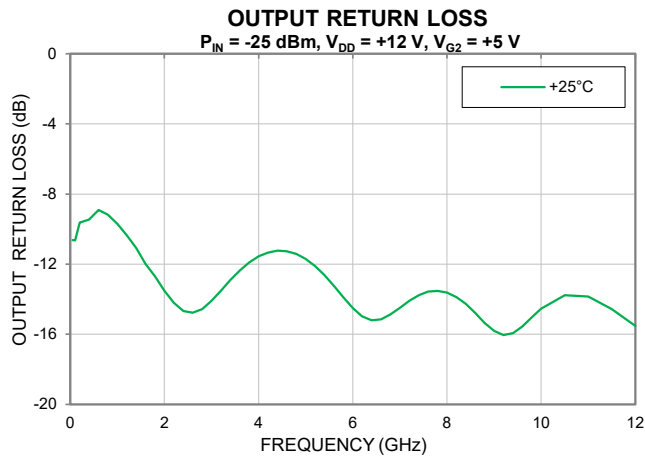
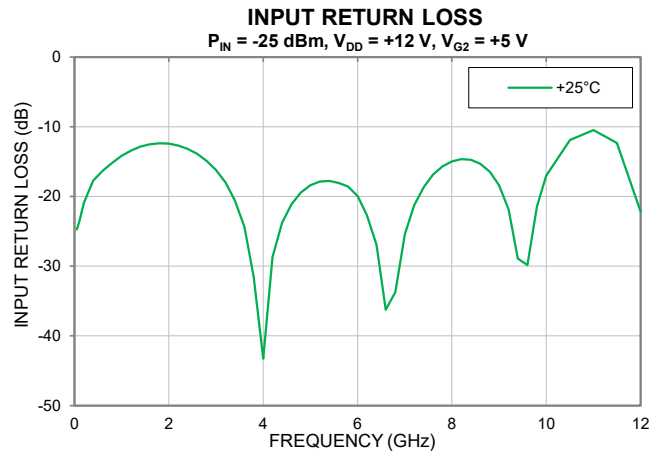
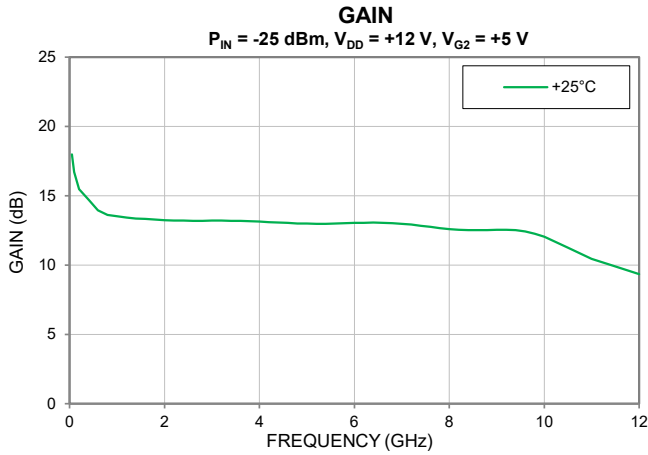
# Power Amplifier

## PMA5-83-2W-D+

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### TYPICAL PERFORMANCE GRAPHS

For additional performance graphs, please see the PMA5-83-2W+ datasheet.





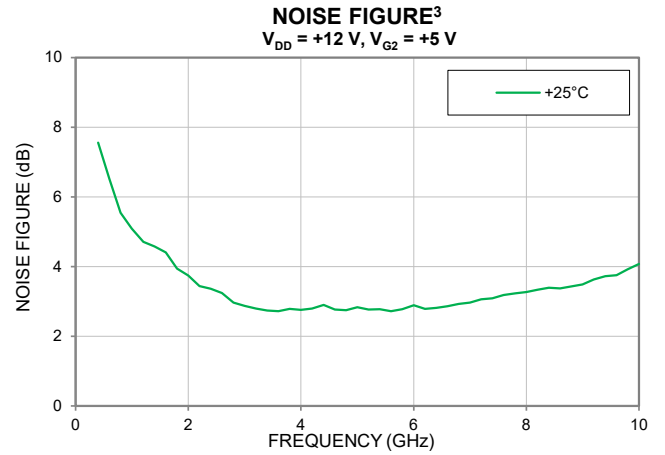
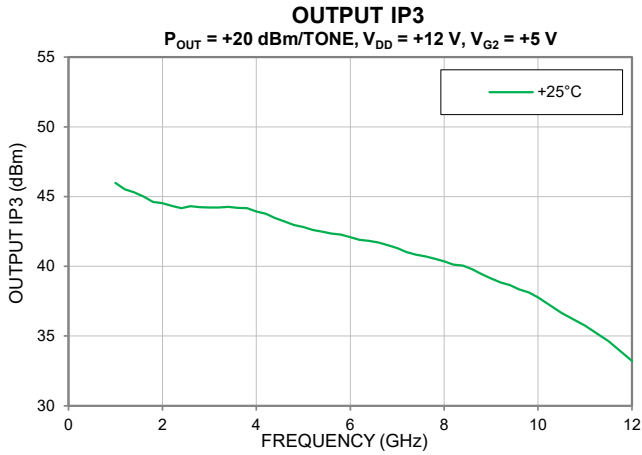
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### TYPICAL PERFORMANCE GRAPHS



3. Noise Figure performance taken from packaged version of amplifier, PMA5-83-2W+.



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## PMA5-83-2W-D+

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### ABSOLUTE MAXIMUM RATINGS<sup>6</sup>

Parameter	Ratings
Operating Temperature <sup>7</sup>	-45°C to +85°C
Storage Temperature (for Die) <sup>8</sup>	-65°C to +150°C
Junction Temperature <sup>9</sup>	+175°C
Total Power Dissipation	10 W
Input Power (CW), V <sub>DD</sub> =+12 V	+31 dBm
DC Voltage at RF-OUT + V <sub>DD</sub>	+16.5 V
Gate Voltage at V <sub>G1</sub>	-0.2 V
Gate Voltage at V <sub>G2</sub>	+7.5 V
DC Gate Current at V <sub>G1</sub> (I <sub>G1</sub> )	4.5 mA
DC Gate Current at V <sub>G2</sub> (I <sub>G2</sub> )	4.5 mA

6. Permanent damage may occur if these limits are exceeded. Maximum ratings are not intended for continuous normal operation.

7. Bottom of Die

8. For die shipped in Gel-Pak see ENV-80 (limited by packaging)

9. Peak temperature on top of Die.

### THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ <sub>jc</sub> ) <sup>10</sup>	6°C/W

10. Θ<sub>jc</sub> = (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

### ESD RATING<sup>11</sup>

	Class	Voltage Range	Reference Standard
HBM	1A	250 V to < 500 V	ANSI/ESDA/JEDEC JS-001-2017
CDM	C2	500 V to < 1000 V	JESD22-C101F



ESD HANDLING PRECAUTION: This device is designed to be Class 1A for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.

11. Tested in 5x5 mm 32-Lead QFN-Style Package





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## FUNCTIONAL DIAGRAM

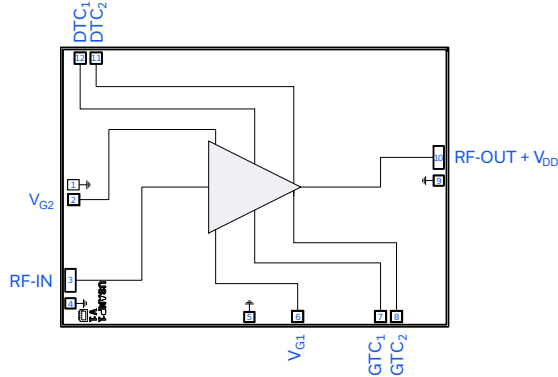


Figure 1. PMA5-83-2W-D+ Functional Diagram

## PAD DESCRIPTION

Function	Pad Number	Description (Refer to Figure 1)
RF-IN	3	RF-IN Pad connects to RF Input port.
RF-OUT + V <sub>DD</sub>	10	RF-OUT Pad connects to RF Output and V <sub>DD</sub> port
V <sub>G1</sub>	6	Gate 1 control voltage.
V <sub>G2</sub>	2	Gate 2 control voltage.
DTC <sub>1</sub>	12	Drain Low Frequency Termination Capacitor (AC GND)
DTC <sub>2</sub>	11	Drain Low Frequency Termination Capacitor (AC GND)
GTC <sub>1</sub>	7	Gate Low Frequency Termination Capacitor (AC GND)
GTC <sub>2</sub>	8	Gate Low Frequency Termination Capacitor (AC GND)
GND	1, 4, 5, 9, & Bottom of Die	Connects to ground.

## DIE OUTLINE: inches [mm], Typical

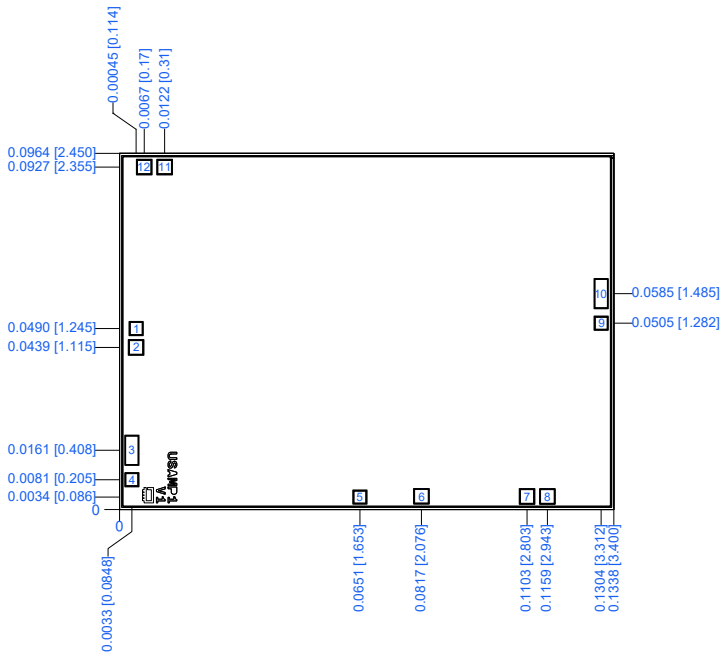


Figure 2. PMA5-83-2W-D+ Outline Drawing.

## DIMENSIONS: inches [mm], Typical

Die Size	0.1338 x 0.0964 [3.400 x 2.450]
Die Thickness	0.0040 [0.100]
Bond Pad Sizes:	
Pads 1, 4, 5, 9	0.0035 x 0.0035 [0.09 x 0.09]
Pads 2, 6, 7, 8, 11, 12	0.0039 x 0.0039 [0.1 x 0.1]
Pads 3, 10	0.0035 x 0.0079 [0.09 x 0.2]
Plating (Pads & Bottom of Die)	Gold





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### CHARACTERIZATION BOARD

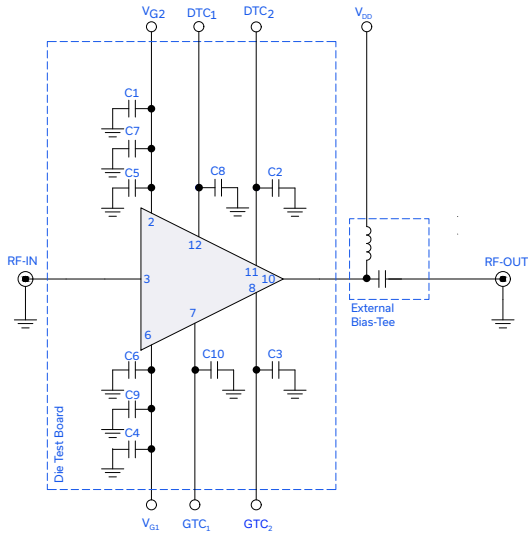


Figure 3. Die Characterization Board

#### Electrical Parameters and Conditions

Gain, Return Loss, Output Power at 1 dB Compression (P1dB), Output IP3 (OIP3), and Noise Figure measured using N5247B PNA-X Microwave Network Analyzer. Device bias voltage V<sub>DD</sub> supplied by external Bias-Tee.

#### Conditions:

Gain and Return Loss: P<sub>IN</sub> = -25 dBm

Output IP3 (OIP3): Two tones, spaced 1 MHz apart, +20 dBm/tone at output.

#### Power ON/Power OFF Sequence

Caution: Permanent damage to the device will occur if the Power ON and Power OFF Sequences

#### Power ON:

1. Set V<sub>G1</sub> = -2 V and Turn ON.
2. Set V<sub>G2</sub> = +5 V and Turn ON.
3. Set V<sub>DD</sub> = +12 V and Turn ON.
4. Increase V<sub>G1</sub> to desired I<sub>bD</sub>.
5. Turn ON RF Signal.

#### Power OFF:

1. Turn OFF RF Signal.
2. Decrease V<sub>G1</sub> to -2 V.
3. Turn OFF V<sub>DD</sub>.
4. Turn OFF V<sub>G2</sub>.
5. Turn OFF V<sub>G1</sub>.

Component	Value	Size	Part Number	Manufacturer
C1, C2, C3, C4	4.7 μF	1206	12063C475KAT2A	AVX CORPORATION
C5	100 pF	0.022x0.022	MA4M3100	MACOM
C6	100 pF	0402	GCM1555C1H101JA16D	MURATA
C7, C8, C9, C10	1000 pF	0402	GCM155R71H102KA37D	MURATA





## ASSEMBLY DIAGRAM

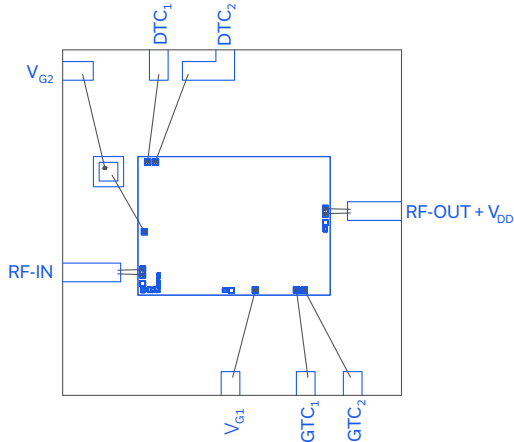



Figure 4. PMA5-83-2W-D+ Assembly Diagram

Refer to the table in Figure 2 for more details on the passive components.

- Bond wire diameter: 1 mil
- Bond wire lengths from Die Pad to PCB at RF-IN & RF-OUT ports:  $22 \pm 2$  mils
- Typical Gap from Die edge to launcher edge: 10 mils
- PCB thickness and material: 8 mil RO4003C (Thickness: 1 oz copper on each side).

## ASSEMBLY AND HANDLING PROCEDURE

1. Storage  
Die should be stored in a dry nitrogen purged desiccator or equivalent.
2.  ESD Precautions  
MMIC pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment  
Devices require careful handling using tools appropriate for manipulating semiconductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The surface of the chips have exposed air bridges and should not be touched with a vacuum collet, tweezers or fingers. The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is ATROX 800HT5 or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding  
Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire. Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance.



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ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASHBOARD [CLICK HERE](#)

<b>Performance Data &amp; Graphs</b>	Data Graphs S-Parameter (S2P Files) Data Set (.zip file)								
<b>Case Style</b>	Die								
<b>RoHS Status</b>	Compliant								
<b>Die Ordering and Packaging Information</b>	<table border="0"> <tr> <td>Quantity, Package</td> <td>Model No.</td> </tr> <tr> <td>Gel - Pak: 5, 10, 50 KGD*</td> <td>PMA5-83-2W-DG+</td> </tr> <tr> <td>Medium<sup>†</sup>, Partial wafer: KGD* &lt; 300</td> <td>PMA5-83-2W-DP+</td> </tr> <tr> <td>Full wafer<sup>†</sup></td> <td>PMA5-83-2W-DF+</td> </tr> </table> <sup>†</sup> Available upon request contact sales representative. Refer to <a href="#">AN-60-067</a>	Quantity, Package	Model No.	Gel - Pak: 5, 10, 50 KGD*	PMA5-83-2W-DG+	Medium <sup>†</sup> , Partial wafer: KGD* < 300	PMA5-83-2W-DP+	Full wafer <sup>†</sup>	PMA5-83-2W-DF+
Quantity, Package	Model No.								
Gel - Pak: 5, 10, 50 KGD*	PMA5-83-2W-DG+								
Medium <sup>†</sup> , Partial wafer: KGD* < 300	PMA5-83-2W-DP+								
Full wafer <sup>†</sup>	PMA5-83-2W-DF+								
<b>Die Marking</b>	USAMP1 V1								
<b>Environmental Ratings</b>	ENV80								

\*Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a higher degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

Notes

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