



MMIC DIE

Voltage Variable Attenuator **PVA-453-34-D+**

Mini-Circuits

50Ω 10 to 45 GHz

THE BIG DEAL

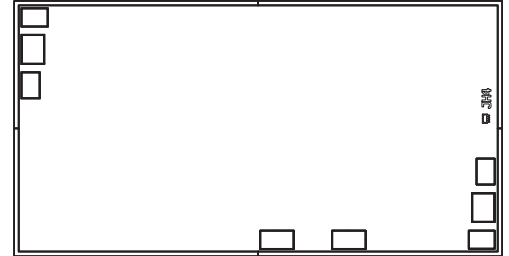
- Ultra-broad band, 10 to 45 GHz
- Wide attenuation range, up to 51 dB typ at 30 GHz
- Excellent return loss for all attenuation states
- Low insertion loss, 2 dB typ
- High IIP3 in all attenuation states

APPLICATIONS

- 5G MIMO and Back Haul Radio Systems
- Satellite Communications
- Test and Measurement Equipment
- Radar, EW, and ECM Defense Systems

PRODUCT OVERVIEW

The PVA-453-34-D+ is an absorptive voltage variable attenuator MMIC die fabricated using GaAs pHEMT technology. This VVA covers the frequency range of 10 to 45 GHz offering high dynamic range, low distortion, and low insertion loss. It features two independently controlled attenuators using analog control voltages from -4V to 0V. This product is ideal for applications where a DC voltage is utilized to control RF signal levels such as temperature compensation and AGC circuits.



+RoHS Compliant

The +Suffix identifies RoHS Compliance.
See our website for methodologies and qualifications

SEE ORDERING INFORMATION ON THE LAST PAGE

KEY FEATURES

Features	Advantages
High IIP3, +26 to +43 dBm typ. over attenuation range	Low distortion enabling improved system performance
Wide attenuation range, <ul style="list-style-type: none"> • 45 dB typ. at 20 GHz • 51 dB typ. at 30 GHz • 38 dB typ. at 40 GHz 	Low insertion loss and high dynamic range simplify the use of analog signal control.



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ELECTRICAL SPECIFICATIONS AT 25°C, 50Ω, UNLESS NOTED OTHERWISE²

Frequency (GHz)	Condition ¹	Min Attenuation (dB) ³ Typ.	Max Attenuation (dB) Typ.	Attenuation Range (dB) Typ.	Return Loss (dB) Typ.	IIP3 (dBm) Worst Case, Typ.
10-20	VCTL1 = -4 V to 0 V, VCTL2 = -4 V	2.1	23.8	21.7	17	30
20-30		2.2	27.6	25.4	14	
30-40		3.0	31.1	28.1	16	
40-45		4.1	34.0	29.9	19	
10-20	VCTL1 = 0 V, VCTL2 = -4 V to 0 V	23.8	41.6	17.7	14	30
20-30		27.6	51.9	24.3	13	
30-40		31.2	48.0	16.8	15	
40-45		34.0	38.0	4.0	18	
10-20	VCTL1 = -4 V to 0 V, VCTL2 = -4 V to 0 V VCTL1 = VCTL2	2.1	41.5	39.5	17	26
20-30		2.2	51.9	49.7	14	
30-40		3.0	48.0	45.0	16	
40-45		4.1	38.0	33.9	19	

1. VCTL1 and VCTL2: -4V (min. attenuation) to 0V (max. attenuation). Maximum current for VCTL1 or VCTL2: 5 mA (max at VCTL= -4V)

2. Tested in industry standard 3.5x2.5 mm, 16-lead MCLP package.

3. Min attenuation state is the insertion loss.

MAXIMUM RATINGS⁴

Parameter	Ratings
Operating Case Temperature	-40°C to 85°C
Control Voltage (Vctl1/Vctl2)	-5 to +1V
Absolute Max. RF Input Level	+23 dBm
Junction Temperature	150°C
Thermal Resistance at max. attenuation	44.8°C/W

4. Permanent damage may occur if any of these limits are exceeded.

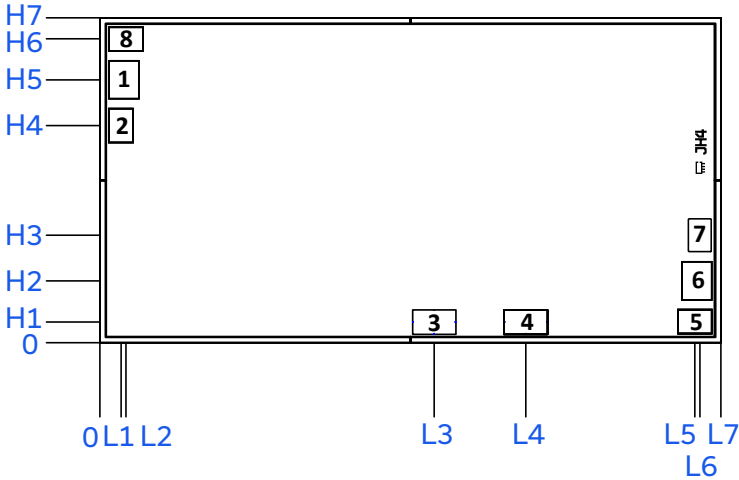


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BONDING PAD POSITION / DESCRIPTION



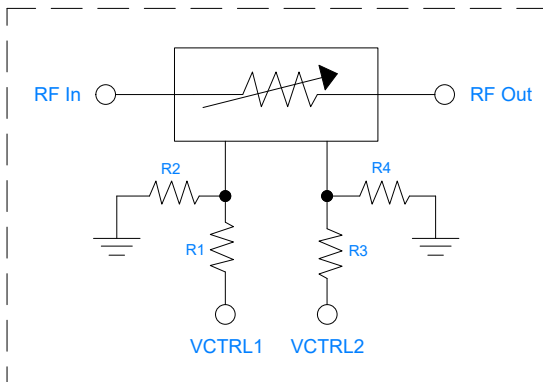
Function	Pad Number	Description
RF-IN	1	RF Input Pad
GROUND	2,5,7,8	Ground
VCTL1	3	Control Voltage 1
VCTL2	4	Control Voltage 2
RF OUT	6	RF Output Pad

- 1. Bond Pad material - Gold
- 2. Bottom of Die - Gold plated

DIMENSION IN μm , TYP.

L1	L2	L3	L4	L5	L6	L7	H1	H2	H3	H4	H5	H6	H7
77.0	96.0	1231.0	1568.0	2190.0	2209.0	2286.0	76.0	228.0	396.0	800.0	968.0	1118.0	1196.0
Thickness	Die Size	Pad Size 1 & 6	Pad Size 2 & 7	Pad Size 3 & 4	Pad Size 5 & 8								
100	2286 x 1196	100 x 130	78 x 115	150 x 80	115 x 78								

APPLICATION CIRCUIT AND PAD DESCRIPTION



RECOMMENDED WIRE LENGTH AND LOOP HEIGHT, TYP.

Wire	Wire Length (mils)	Wire Loop Height (mils)
RF-IN	12	7
RF-OUT	12	7
VCTL1 AND VCTL2	Not Critical	

Components	Size	Value	Qty	Part Number
R1, R3	0201	6.2 kΩ	2	RK73414TTC6201F
R2, R4	0201	2.1 kΩ	2	RK73H1HT2010F



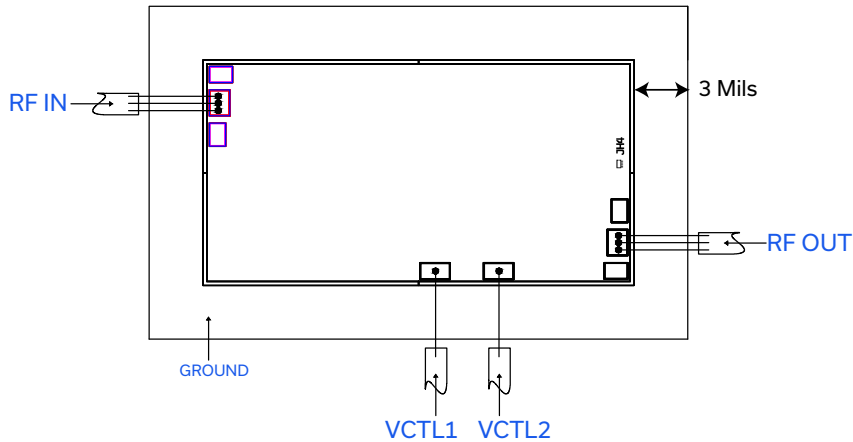
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ASSEMBLY DIAGRAM



ASSEMBLY PROCEDURE

- Storage**
Die should be stored in a dry nitrogen purged desiccators or equivalent.
- ESD**
 MMIC voltage variable attenuator die are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be open in clean room conditions at an appropriately grounded anti-static workstation.
- Die Handling and Attachment**
Devices need careful handling using correctly designed collets, it is recommended to handle the chip along the edges with a custom design collet. The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are Ablestik 84-1 LMISR4 or equivalents. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. The surface of the chip has exposed air bridges and should not be touched with vacuum collet, tweezers or fingers.
- Wire Bonding**
Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the die gold bond pads. Thermo-sonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1mil diameter. Bonds must be made from the bond pads on the die to the packaged or substrate. All bond wires should be kept as short as low as reasonable to minimize performance degradation due to undesirable series inductance.



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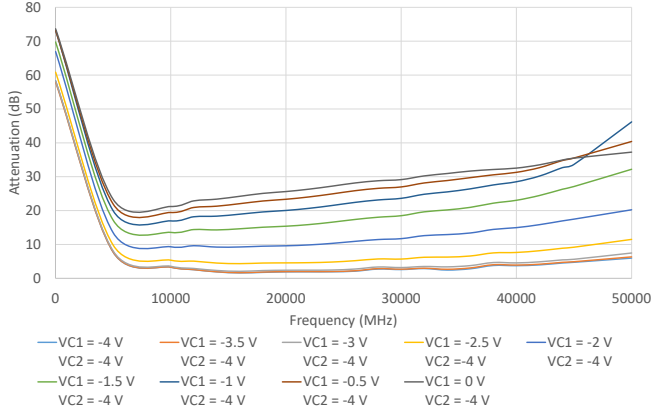
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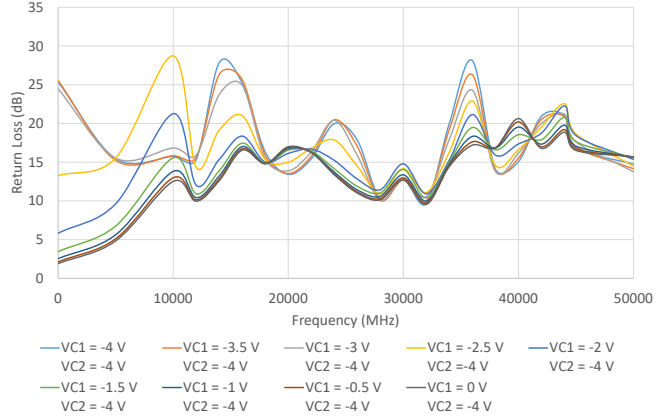
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TYPICAL PERFORMANCE CURVES

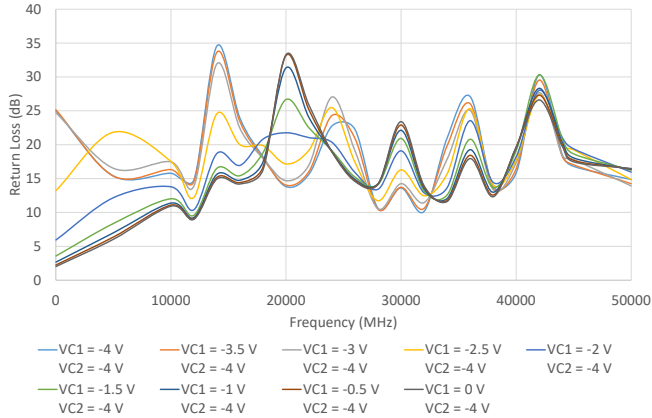
Attenuation vs. Frequency at Various Control Voltages
VCTRL 1 = -4 V to 0 V, VCTRL 2 = -4 V



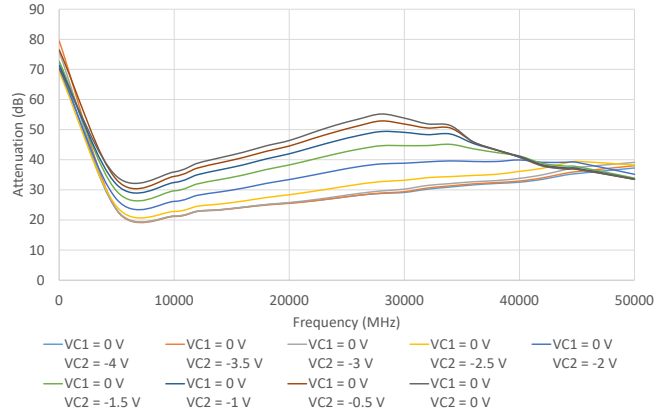
Input Return Loss vs. Frequency at Various Control Voltages
VCTRL 1 = -4 V to 0 V, VCTRL 2 = -4 V



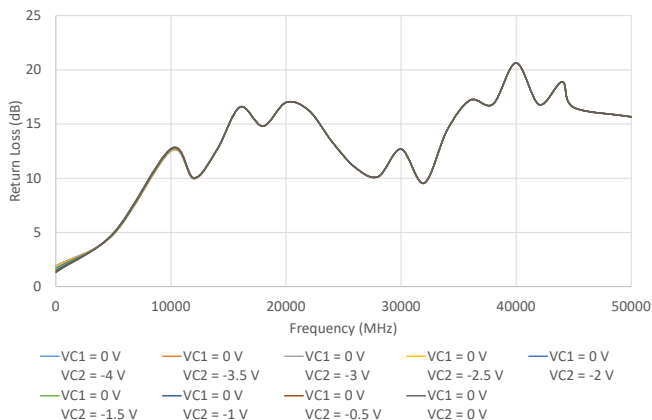
Output Return Loss vs. Frequency at Various Control Voltages
VCTRL 1 = -4 V to 0 V, VCTRL 2 = -4 V



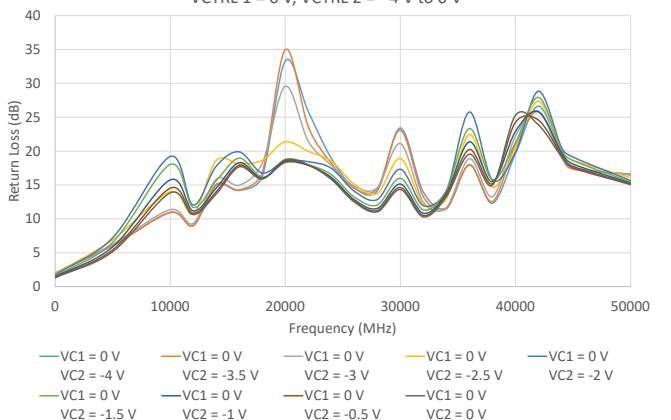
Attenuation vs. Frequency at Various Control Voltages
VCTRL 1 = 0 V, VCTRL 2 = -4 V to 0 V



Input Return Loss vs. Frequency at Various Control Voltages
VCTRL 1 = 0 V, VCTRL 2 = -4 V to 0 V



Output Return Loss vs. Frequency at Various Control Voltages
VCTRL 1 = 0 V, VCTRL 2 = -4 V to 0 V





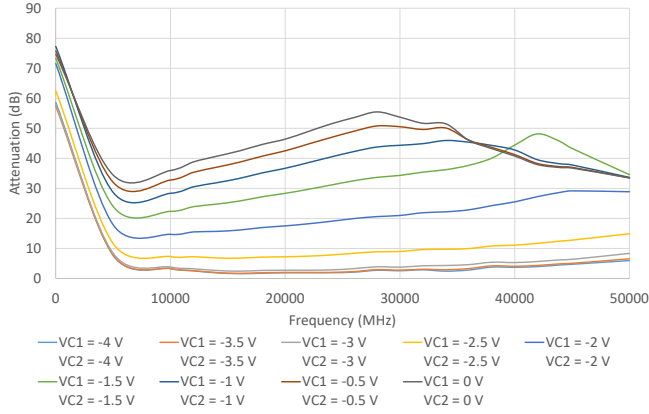
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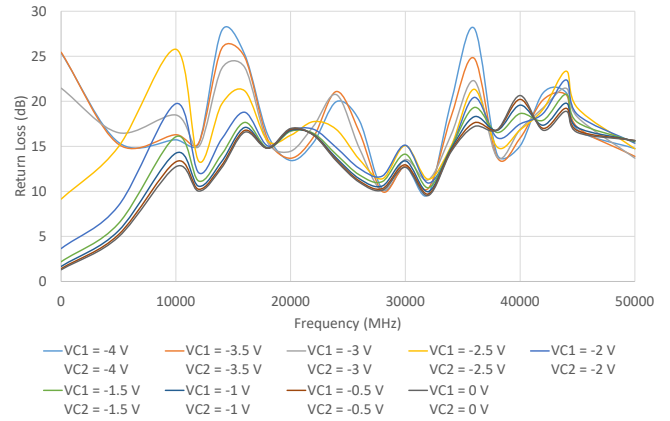
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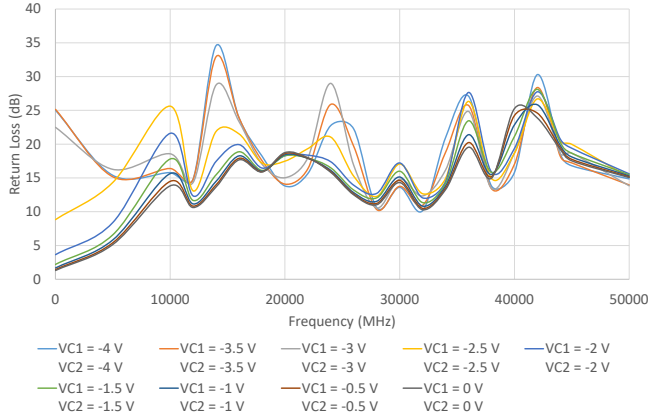
Attenuation vs. Frequency at Various Control Voltages
VCTRL1 = VCTRL2 = -4 V to 0 V



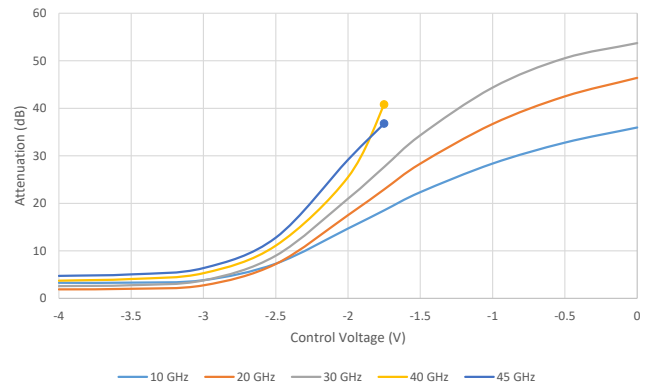
Input Return Loss vs. Frequency at Various Control Voltages
VCTRL1 = VCTRL2 = -4 V to 0 V



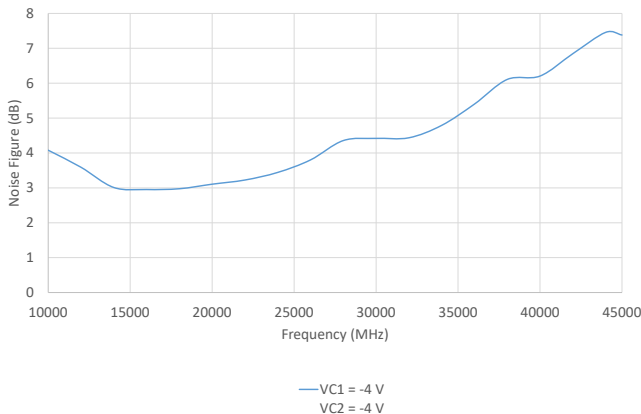
Output Return Loss vs. Frequency at Various Control Voltages
VCTRL1 = VCTRL2 = -4 V to 0 V



Attenuation vs. Control Voltage at Various Frequencies
(VCTRL1 = VCTRL2)



Noise Figure vs. Frequency





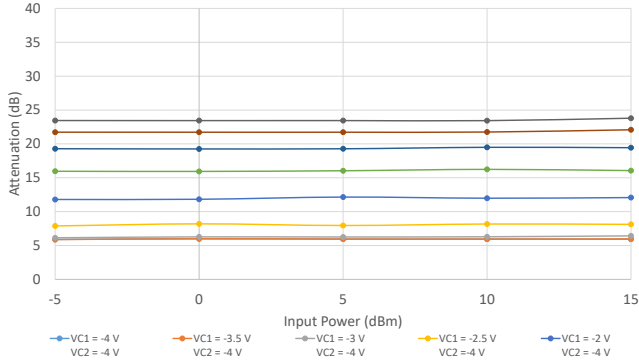
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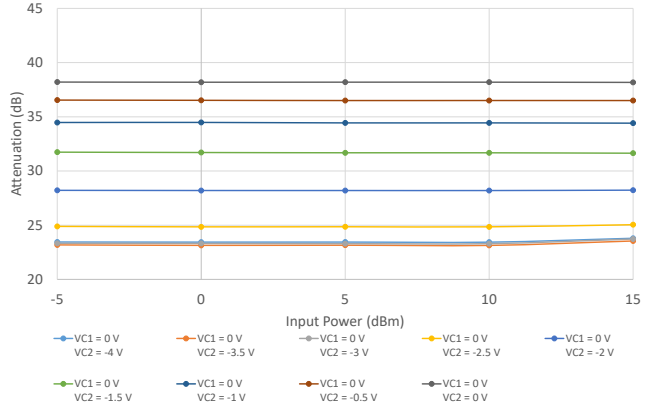
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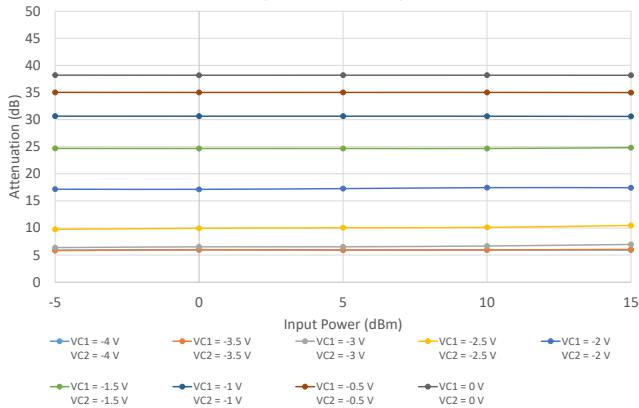
Attenuation vs. Input Power Over Control Voltages at 10 GHz
(Fixed VCTRL2)



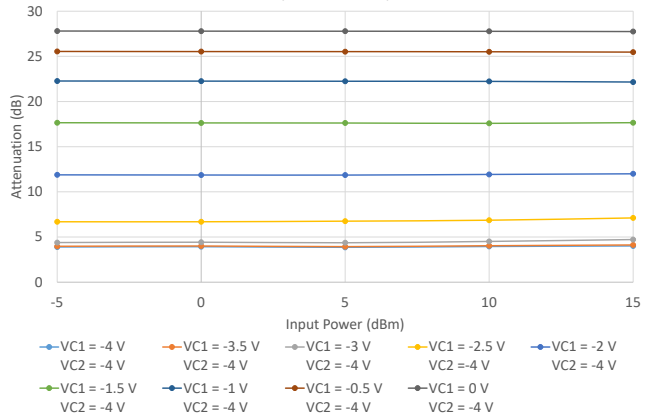
Attenuation vs. Input Power Over Control Voltages at 10 GHz
(Fixed VCTRL1)



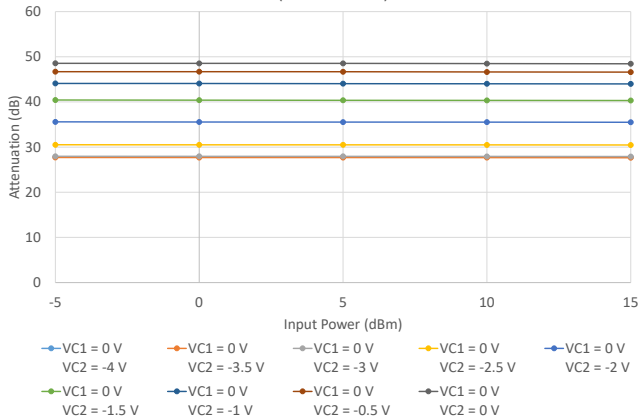
Attenuation vs. Input Power Over Control Voltages at 10 GHz
(VCTRL1 = VCTRL2)



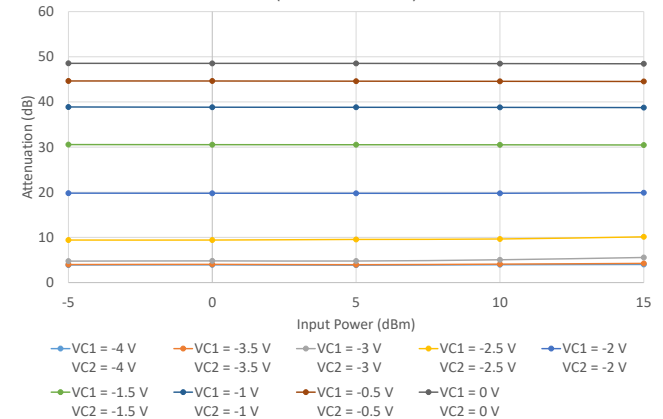
Attenuation vs. Input Power Over Control Voltages at 20 GHz
(Fixed VCTRL2)



Attenuation vs. Input Power Over Control Voltages at 20 GHz
(Fixed VCTRL1)



Attenuation vs. Input Power Over Control Voltages at 20 GHz
(VCTRL1 = VCTRL2)





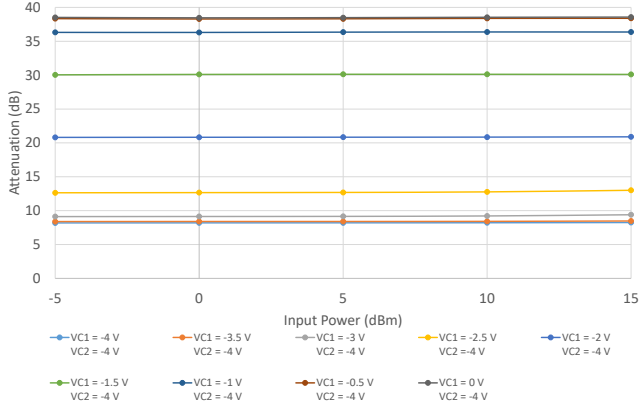
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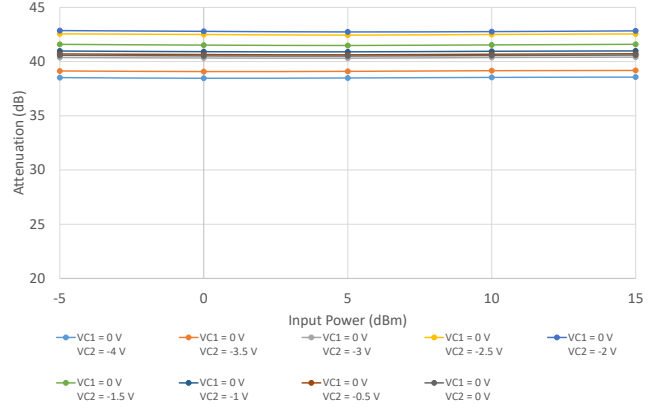
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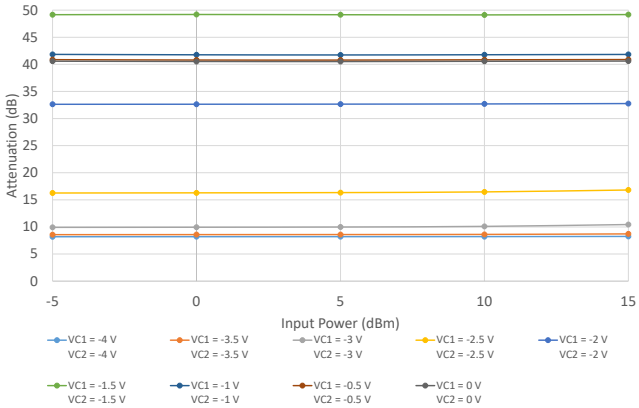
Attenuation vs. Input Power Over Control Voltages at 44 GHz (Fixed VCTRL2)



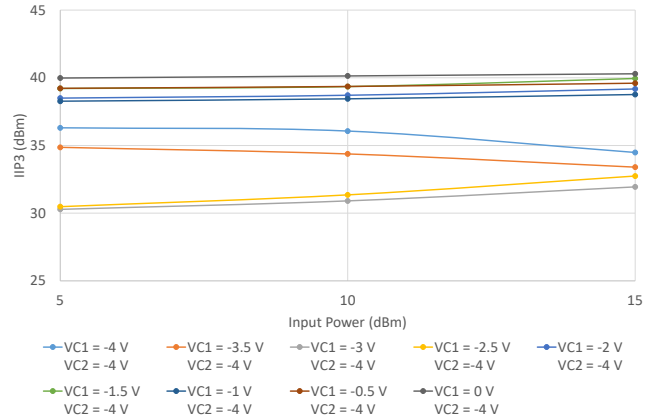
Attenuation vs. Input Power Over Control Voltages at 44 GHz (Fixed VCTRL1)



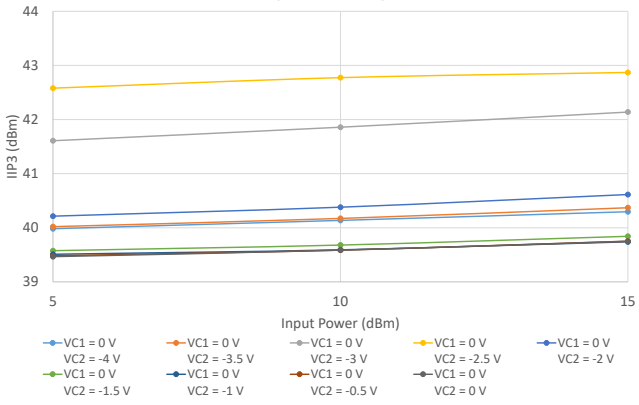
Attenuation vs. Input Power Over Control Voltages at 44 GHz (VCTRL1 = VCTRL2)



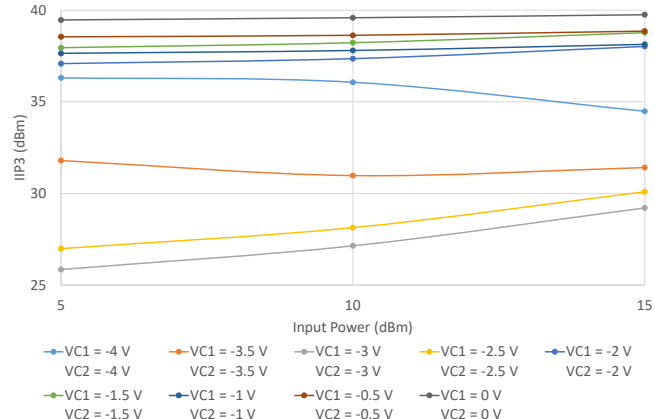
IIP3 vs. Input Power Over Control Voltages at 10 GHz (Fixed VCTRL2)



IIP3 vs. Input Power Over Control Voltages at 10 GHz (Fixed VCTRL1)



IIP3 vs. Input Power Over Control Voltages at 10 GHz (VCTRL1 = VCTRL2)





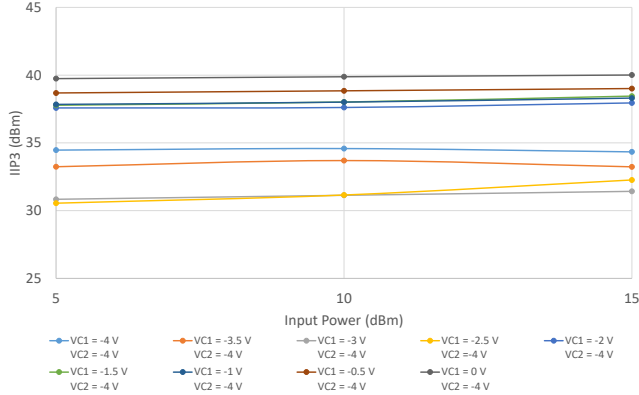
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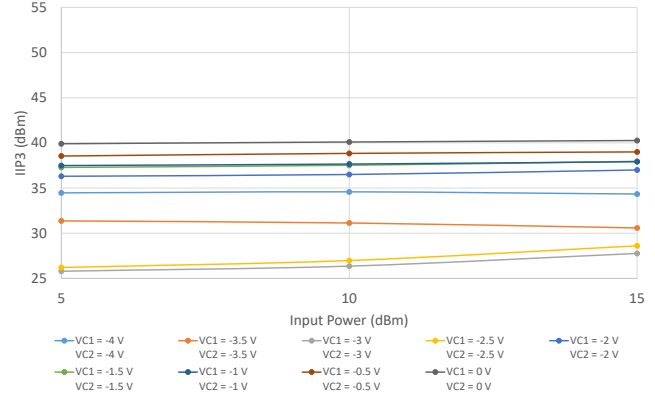
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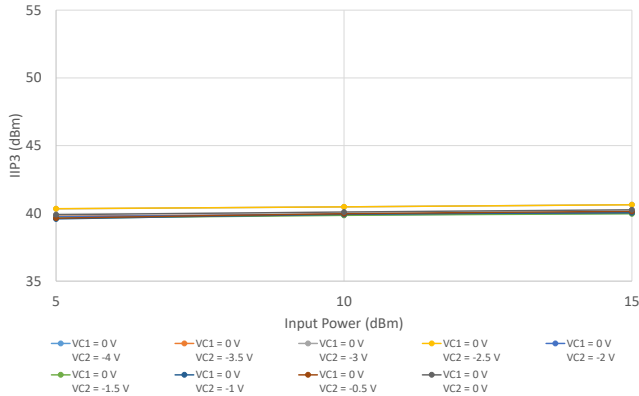
IIP3 vs. Input Power Over Control Voltages at 20 GHz (Fixed VCTRL2)



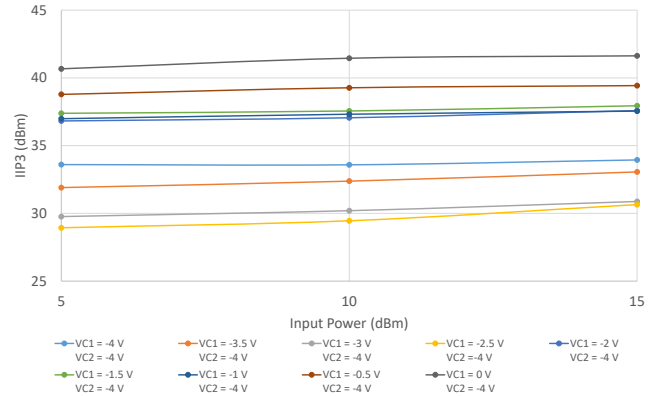
IIP3 vs. Input Power Over Control Voltages at 20 GHz (VCTRL1 = VCTRL2)



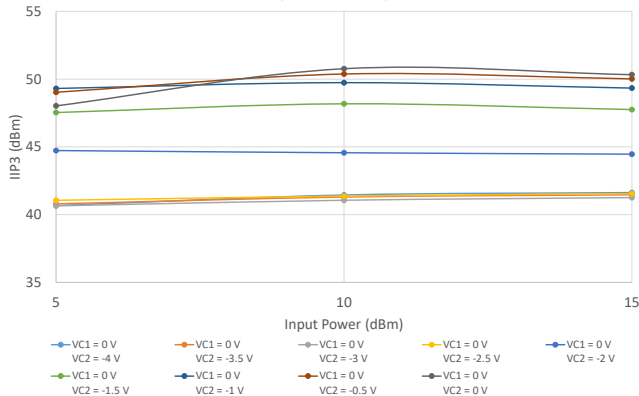
IIP3 vs. Input Power Over Control Voltages at 20 GHz (Fixed VCTRL1)



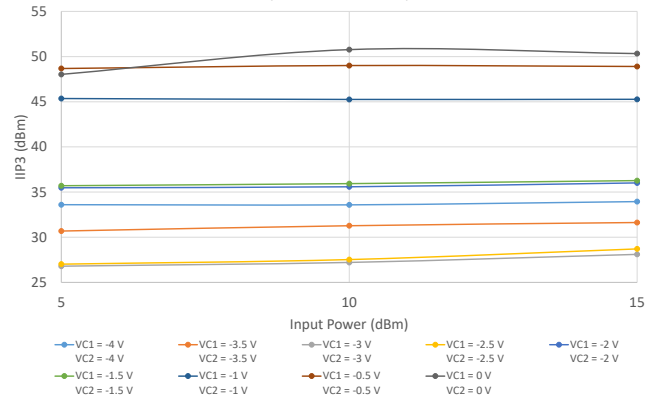
IIP3 vs. Input Power Over Control Voltages at 44 GHz (Fixed VCTRL2)



IIP3 vs. Input Power Over Control Voltages at 44 GHz (Fixed VCTRL1)



IIP3 vs. Input Power Over Control Voltages at 44 GHz (VCTRL1 = VCTRL2)





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ADDITIONAL DETAILED TECHNICAL INFORMATION IS AVAILABLE ON OUR DASH BOARD.

Performance Data	Data Table	
	Swept Graphs	
	S-Parameter (S2P Files) Data Set with and without port extension(.zip file)	
Case Style	Die	
Die Ordering and packaging information	Quantity, Package Small, Gel - Pak: 5,10,50,100 KGD* Medium†, Partial wafer: KGD*<714 Large†, Full Wafer	Model No. PVA-453-34-DG+ PVA-453-34-DP+ PVA-453-34-DF+
	†Available upon request contact sales representative	
Die Marking	JH4	
Environmental Ratings	ENV80	

*Known Good Die ("KGD") means that the die are taken from PCM good wafer and then visually inspected per Mini-Circuits' criteria. Though this is not definitive, it does provide a higher degree of confidence that the die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

ESD RATING**

Human Body Model (HBM): Class 1A (250 V to < 500 V) in accordance with ANSI/ESD STM5.1-2001

** Tested in industry standard 2.5x3.5 mm, 16-lead MCLP Package.

NOTES

- A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
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