MMIC DIE

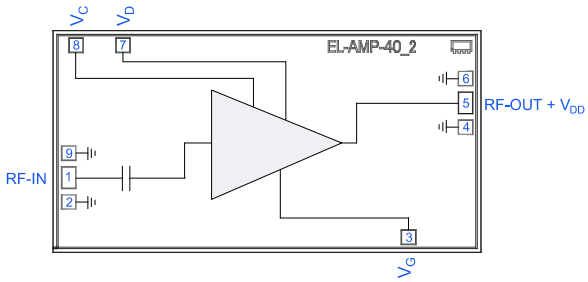
Variable Gain Amplifier PVGA-273-D+

50Ω 0.3 to 26.5 GHz High Dynamic Range

THE BIG DEAL

- Wide Bandwidth, 0.3 to 26.5 GHz
- Output P1dB, Typ. +17.3 dBm
- High OIP3, Typ. +29 dBm
- Adjustable Gain Range, Typ. 30 dB
- Supply Voltage, +5 V or +8 V

FUNCTIONAL DIAGRAM



SEE ORDERING INFORMATION ON THE LAST PAGE

APPLICATIONS

- Test and Measurement Equipment
- Radar, EW, and ECM Defense Systems
- 5G MIMO and Back Haul Radio Systems
- Signal Distribution Networks

PRODUCT OVERVIEW

Mini-Circuits' PVGA-273-D+ is a low noise variable gain MMIC amplifier fabricated in GaAs pHEMT technology. Operating from 0.3 to 26.5 GHz, this amplifier features a high dynamic range with 2.1 dB noise figure, 15.7 dB gain, +17.3 dBm P1dB, and +29 dBm OIP3. This design has the flexibility to operate from a +8 V drain voltage applied directly to the device or a +5 V drain voltage applied via a bias tee through the output port. An additional, optional supply voltage may be applied to enable a gain control range of 30 dB.

KEY FEATURES

Features	Advantages
Wide Bandwith, 0.3 to 26.5 GHz • 17.5 dB Typ. Gain at 1 GHz • 14.1 dB Typ. Gain at 26.5 GHz	Suitable for wide bandwidth defense and test and measurement applications, as well as narrowband performance-driven applications.
High P1dB & OIP3 • +17.3 dBm Typ. P1dB • +29 dBm Typ. OIP3	Suitable as a driver amplifier in receiver/transmitter chains due to high linearity with low dissipated power.
Adjustable Gain Range • 30 dB	Enables temperature compensation and power control for transmit and receive signal chains.
Unpackaged Die	Enables integration into hybrid chip and wire assemblies.

REV. OR
ECO-021313
PVGA-273-D+
MCL NY
240326

Variable Gain Amplifier PVGA-273-D+

50Ω 0.3 to 26.5 GHz High Dynamic Range

ELECTRICAL SPECIFICATIONS[1] AT +25°C, V_C = OPEN, UNLESS NOTED OTHERWISE

Parameter	Frequency (GHz)	V_{DD} = +5 V (Applied at RF-OUT)			V_D = +8 V (Applied at Pin 2)[2]			Units
		Min.	Typ.	Max	Min.	Typ.	Max	
Frequency Range		0.3		26.5	0.3		26.5	GHz
Gain	0.3		17.9			16.7		dB
	1.0		17.5			16.7		
	6.0		15.6			14.8		
	12.0		15.7			14.1		
	18.0		15.3			14.3		
	26.5		14.1			13.3		
Output Power at 1 dB Compression (P1dB)	0.3		+17.5			+14.9		dBm
	1.0		+17.8			+15.4		
	6.0		+17.9			+15.7		
	12.0		+17.3			+14.2		
	18.0		+16.1			+13.7		
	26.5		+15.1			+12.1		
Output Power at Saturation (P_{SAT})[3]	0.3		+21.0			+17.9		dBm
	1.0		+20.9			+18.2		
	6.0		+21.0			+18.4		
	12.0		+21.0			+17.3		
	18.0		+19.5			+16.7		
	26.5		+18.9			+16.8		
Output Third-Order Intercept (P_{OUT} = 0 dBm/Tone)	0.3		+28.4			+26.5		dBm
	1.0		+28.9			+27.2		
	6.0		+28.8			+27.7		
	12.0		+28.8			+26.6		
	18.0		+27.7			+26.2		
	26.5		+23.5			+23.1		
Input Return Loss	0.3		5			7		dB
	1.0		8			11		
	6.0		13			13		
	12.0		16			10		
	18.0		24			20		
	26.5		10			17		
Output Return Loss	0.3		14			11		dB
	1.0		13			24		
	6.0		13			12		
	12.0		15			11		
	18.0		13			17		
	26.5		13			14		
Isolation	0.3 - 26.5		36			39		dB
Noise Figure	0.3		4.4			3.9		dB
	1.0		2.7			2.5		
	6.0		2.0			2.0		
	12.0		2.1			2.3		
	18.0		2.6			2.8		
	26.5		4.0			4.2		
Device Operating (V_{DD} or V_D)			+5			+8		V
Device Operating Current (I_{DD} or I_D)[4]			80			80		mA
Gate Voltage (V_G)		-0.46	-0.38	-0.31	-0.45	-0.37	-0.29	V
Gate Current (I_G)			0.02			0.02		mA
Control Voltage (V_C)		-1	Open	+2	-1	Open	+2	V

1. Tested on Mini-Circuits Die Characterization Test Board. See Figure 3.
2. Electrical specifications were measured on packaged model PVGA-273+ on its Mini-Circuits Characterization Test Board TB-PVGA-273C+.
3. P_{SAT} is defined as when the Output Power changes 0.1 dB per 1 dB change in Input Power.
4. Current at P_{IN} = -25 dBm. Increases to 93 mA typical at P1dB (V_{DD} = +5 V) and 86 mA typical at P1dB (V_D = +8 V).

Variable Gain Amplifier PVGA-273-D+

50Ω 0.3 to 26.5 GHz High Dynamic Range

ELECTRICAL SPECIFICATIONS[5] OVER VARIOUS V_C AT +25°C, V_{DD} = +5 V, UNLESS NOTED OTHERWISE

Parameter (Typ.)	Frequency (GHz)	Control Voltage, V_C			Units
		-0.7 V	+1 V	+2 V	
DC Current		23	51	82	mA
Gain	0.3	11.2	16.0	16.8	dB
	1.0	10.8	15.9	16.7	
	6.0	6.6	13.5	14.5	
	12.0	5.4	12.8	13.8	
	18.0	5.0	12.9	14.0	
	26.5	2.5	11.9	13.1	
Output Power at 1 dB Compression (P1dB)	0.3	-2.2	+14.4	+15.5	dBm
	1.0	-2.7	+14.4	+15.8	
	6.0	-4.2	+14.3	+16.0	
	12.0	-3.9	+13.5	+14.9	
	18.0	-3.7	+12.5	+14.1	
	26.5	-3.7	+11.0	+12.6	
Output Power at Saturation (P_{SAT})[6]	0.3	+0.8	+17.3	+18.9	dBm
	1.0	+0.2	+17.7	+19.4	
	6.0	-0.3	+17.6	+19.4	
	12.0	+2.1	+16.9	+18.4	
	18.0	+5.5	+16.1	+17.7	
	26.5	+1.3	+17.7	+19.1	
Output Third-Order Intercept (P_{OUT} = -9 dBm/Tone)	0.3	+5.9	+24.9	+25.9	dBm
	1.0	+5.7	+24.7	+26.4	
	6.0	+4.9	+25.2	+27.4	
	12.0	+5.0	+24.2	+26.2	
	18.0	+4.9	+23.1	+25.4	
	26.5	+5.0	+20.2	+22.0	
Input Return Loss	0.3	4	6	6	dB
	1.0	6	11	11	
	6.0	8	12	13	
	12.0	7	9	10	
	18.0	17	21	19	
	26.5	18	18	19	
Output Return Loss	0.3	13	12	12	dB
	1.0	24	26	25	
	6.0	12	12	12	
	12.0	11	11	11	
	18.0	18	18	18	
	26.5	15	15	15	
Isolation	0.3 – 26.5	33	38	39	dB
Noise Figure	0.3	5.8	4.1	3.9	dB
	1.0	3.3	2.5	2.4	
	6.0	4.1	2.3	2.2	
	12.0	4.4	2.3	2.2	
	18.0	5.2	2.8	2.7	
	26.5	7.1	4.1	4.1	

5. Electrical specification over various V_C was measured on model PVGA-273+ on its Mini-Circuits Characterization Test Board TB-PVGA-273C+.
6. P_{SAT} is defined as when the Output Power changes 0.1 dB per 1 dB change in Input Power.

Variable Gain Amplifier PVGA-273-D+

50Ω 0.3 to 26.5 GHz High Dynamic Range

ELECTRICAL SPECIFICATIONS[7] OVER VARIOUS V_C AT +25°C, V_D = +8 V, UNLESS NOTED OTHERWISE

Parameter (Typ.)	Frequency (GHz)	Control Voltage, V_C			Units
		-0.7 V	+1 V	+2 V	
DC Current		37	58	82	mA
Gain	0.3	15.2	16.2	16.7	dB
	1.0	14.7	16.1	16.7	
	6.0	11.9	14.0	14.8	
	12.0	11.0	13.3	14.1	
	18.0	9.5	13.4	14.2	
	26.5	7.4	12.3	13.2	
Output Power at 1 dB Compression (P1dB)	0.3	+5.9	+14.2	+14.8	dBm
	1.0	+4.8	+14.0	+15.3	
	6.0	+4.0	+14.2	+15.7	
	12.0	+3.4	+13.4	+14.1	
	18.0	+2.6	+12.3	+13.5	
	26.5	+1.0	+11.2	+11.8	
Output Power at Saturation (P_{SAT})[8]	0.3	+8.9	+17.5	+17.9	dBm
	1.0	+8.4	+17.8	+18.3	
	6.0	+8.4	+17.9	+18.4	
	12.0	+8.0	+16.9	+17.3	
	18.0	+8.6	+16.4	+16.7	
	26.5	+7.1	+16.8	+16.5	
Output Third-Order Intercept (P_{OUT} = -9 dBm/Tone)	0.3	+17.2	+26.0	+26.8	dBm
	1.0	+16.7	+25.5	+27.3	
	6.0	+15.4	+25.5	+28.0	
	12.0	+14.1	+24.5	+26.7	
	18.0	+13.5	+24.4	+27.1	
	26.5	+11.4	+21.3	+23.2	
Input Return Loss	0.3	6	6	7	dB
	1.0	9	11	11	
	6.0	11	12	13	
	12.0	9	9	10	
	18.0	20	21	20	
	26.5	17	17	17	
Output Return Loss	0.3	14	12	11	dB
	1.0	19	26	24	
	6.0	11	12	12	
	12.0	11	11	11	
	18.0	18	18	17	
	26.5	15	14	14	
Isolation	0.3 – 26.5	35	38	39	dB
Noise Figure	0.3	7.5	4.7	3.9	dB
	1.0	4.1	2.8	2.5	
	6.0	2.8	2.1	2.1	
	12.0	3.3	2.3	2.3	
	18.0	3.9	2.8	2.8	
	26.5	5.7	4.2	4.3	

7. Electrical specification over various V_C was measured on model PVGA-273+ on it Mini-Circuits Characterization Test Board TB-PVGA-273C+.
8. P_{SAT} is defined as when the Output Power changes 0.1 dB per 1 dB change in Input Power.

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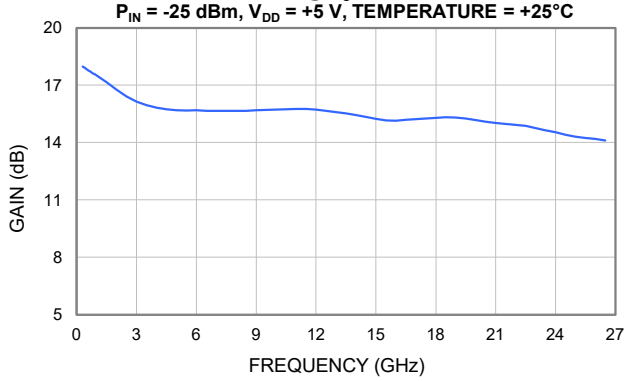
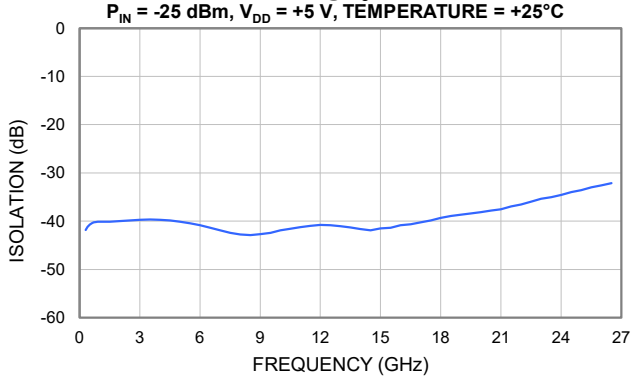
TYPICAL PERFORMANCE GRAPHS WITH V_{DD} = +5 V AND V_D = OPEN

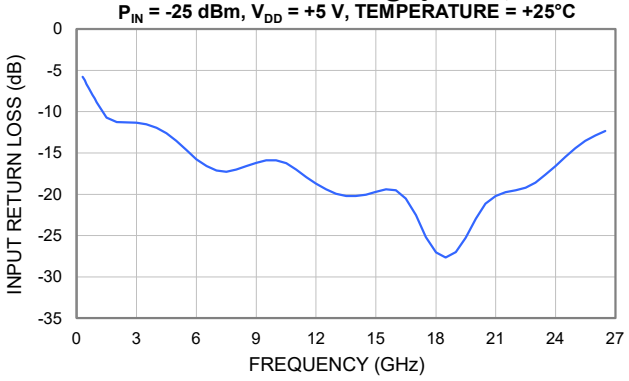
GAIN @ V_C = OPEN,
P_{IN} = -25 dBm, V_{DD} = +5 V, TEMPERATURE = +25°C



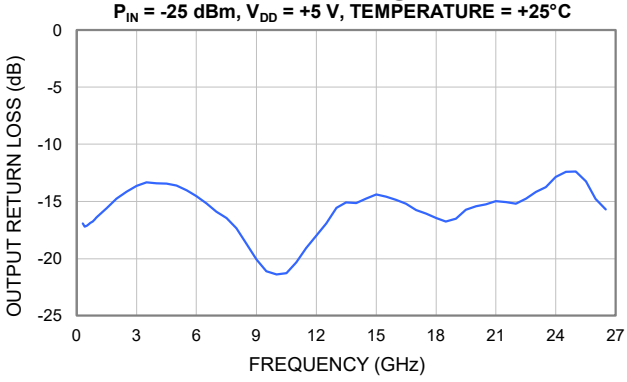
ISOLATION @ V_C = OPEN,
P_{IN} = -25 dBm, V_{DD} = +5 V, TEMPERATURE = +25°C



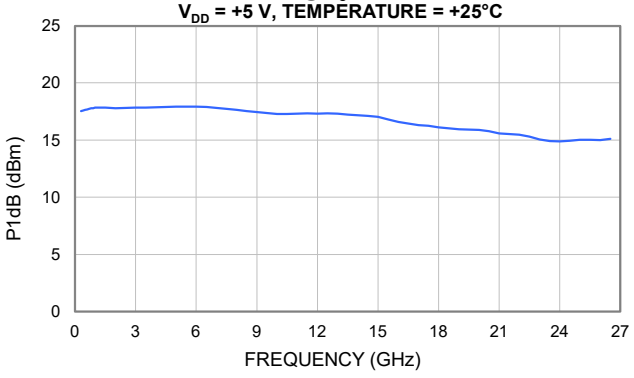
INPUT RETURN LOSS @ V_C = OPEN,
P_{IN} = -25 dBm, V_{DD} = +5 V, TEMPERATURE = +25°C



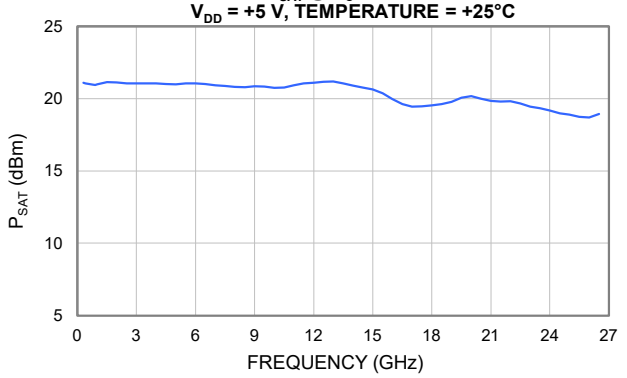
OUTPUT RETURN LOSS @ V_C = OPEN,
P_{IN} = -25 dBm, V_{DD} = +5 V, TEMPERATURE = +25°C



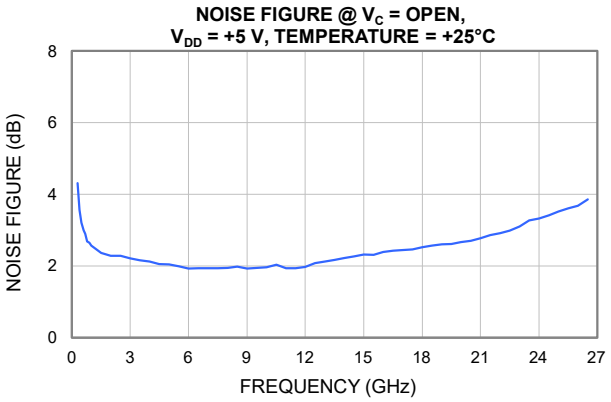
P1dB @ V_C = OPEN,
V_{DD} = +5 V, TEMPERATURE = +25°C



P_{SAT} @ V_C = OPEN,
V_{DD} = +5 V, TEMPERATURE = +25°C

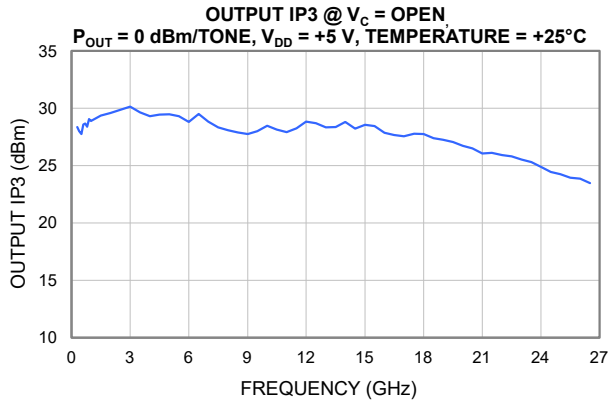


TYPICAL PERFORMANCE GRAPHS WITH V_{DD} = +5 V AND V_D = OPEN



TYPICAL PERFORMANCE GRAPHS WITH V_{DD} = +5 V AND V_D = OPEN

Note: All data in this section represents the Die attached in a 5x5 mm 32-Lead QFN style package and measured on Mini-Circuits Characterization Test Board TB-PVGA-273C+



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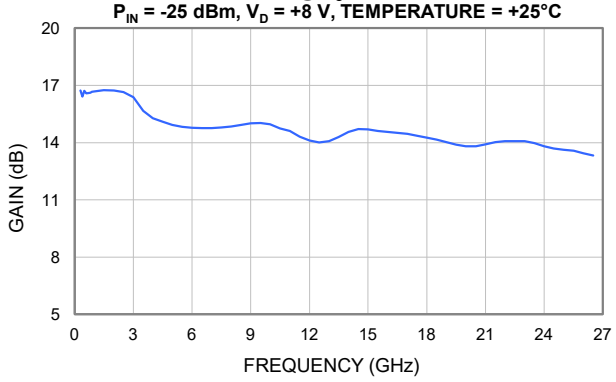
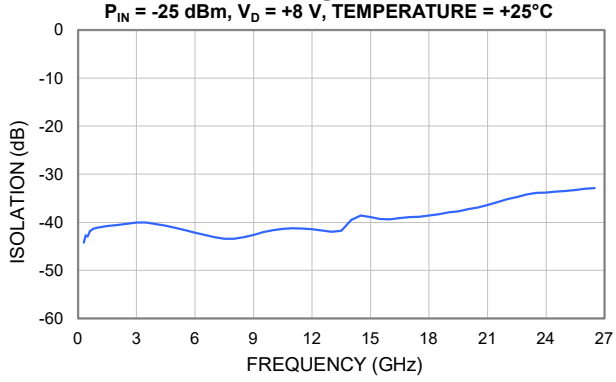
TYPICAL PERFORMANCE GRAPHS WITH V_D = +8 V AND V_{DD} = OPEN

Note: All data on this page represents the Die attached in a 5x5 mm 32-Lead QFN style package and measured on Mini-Circuits Characterization Test Board TB-PVGA-273C+

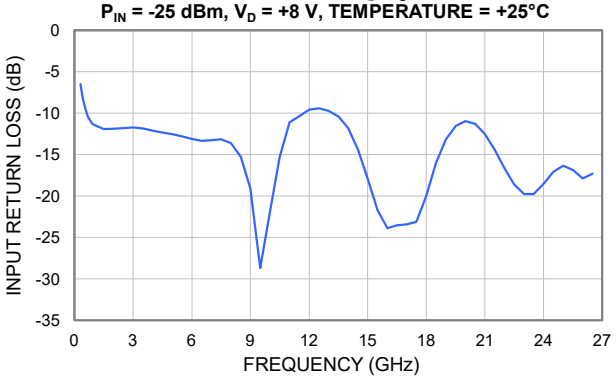
GAIN @ V_C = OPEN,
P_{IN} = -25 dBm, V_D = +8 V, TEMPERATURE = +25°C



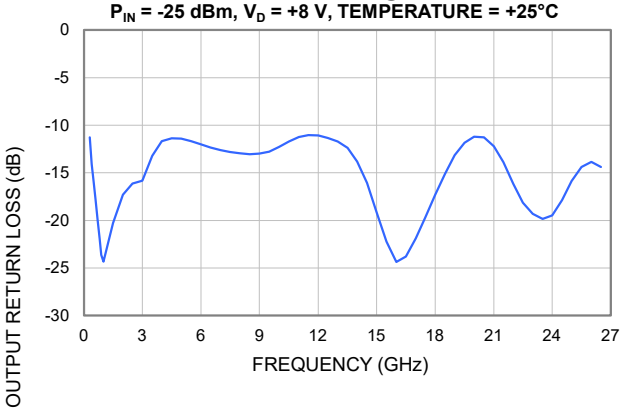
ISOLATION @ V_C = OPEN,
P_{IN} = -25 dBm, V_D = +8 V, TEMPERATURE = +25°C



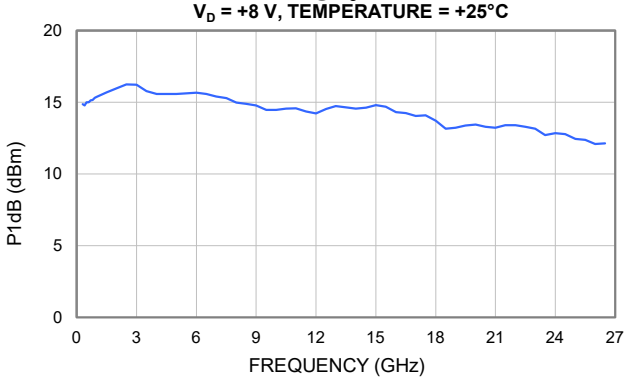
INPUT RETURN LOSS @ V_C = OPEN,
P_{IN} = -25 dBm, V_D = +8 V, TEMPERATURE = +25°C



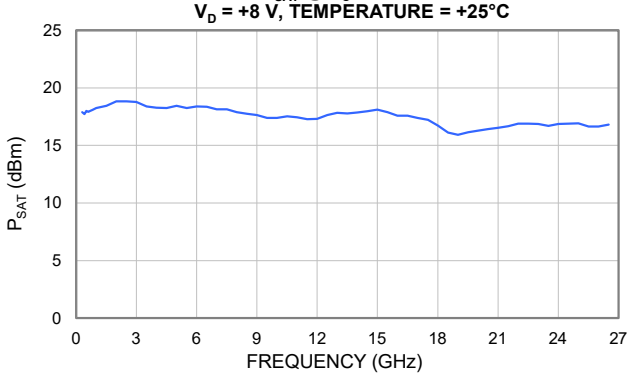
OUTPUT RETURN LOSS @ V_C = OPEN,
P_{IN} = -25 dBm, V_D = +8 V, TEMPERATURE = +25°C



P1dB @ V_C = OPEN,
V_D = +8 V, TEMPERATURE = +25°C



P_{SAT} @ V_C = OPEN,
V_D = +8 V, TEMPERATURE = +25°C

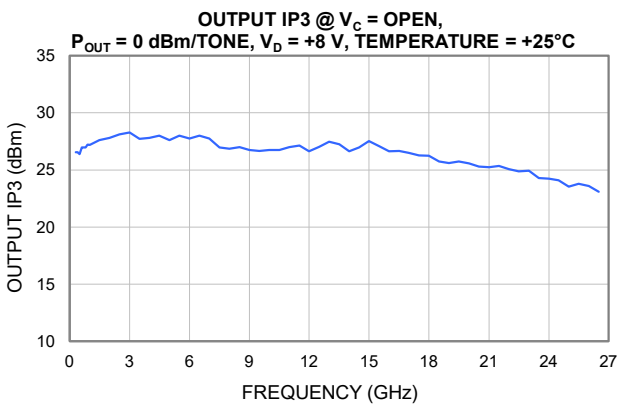


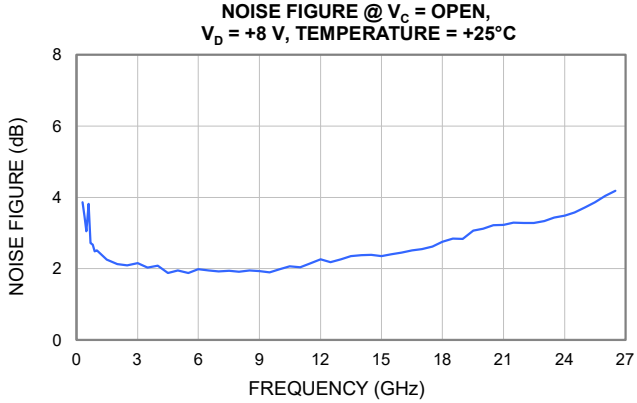
Variable Gain Amplifier PVGA-273-D+

50Ω 0.3 to 26.5 GHz High Dynamic Range

TYPICAL PERFORMANCE GRAPHS WITH V_D = +8 V AND V_{DD} = OPEN

Note: All data on this page represents the Die attached in a 5x5 mm 32-Lead QFN style package and measured on Mini-Circuits Characterization Test Board TB-PVGA-273C+





ABSOLUTE MAXIMUM RATINGS[9]

Parameter	Ratings
Operating Temperature[10]	-45°C to +105°C
Storage Temperature[11]	-65°C to +150°C
Junction Temperature[12]	+150°C
Total Power Dissipation, V_{DD} = +5 V	2.75 W
Total Power Dissipation, V_D = +8 V	2.75 W
Input Power (CW), V_{DD} = +5 V	+24 dBm
Input Power (CW), V_D = +8 V	+24 dBm
DC Voltage on V_{DD}	+11 V
DC Voltage on V_D	+11 V
Current I_{DD}	250 mA
Current I_D	250 mA
DC Voltage on V_G	0 V
Current I_G	0.18 mA
DC Voltage on V_C	+2 V

9. Permanent damage may occur if any of these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
10. Bottom of Die.
11. For Die shipped in Gel-Pak see ENV80 (Limited by packaging).
12. Peak temperature on top of Die.

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ_{JC})[13]	7.2°C/W

13. Θ_{JC}= (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING[14]

	Class	Voltage Range	Reference Standard
HBM	1A	250 V to <500V	ANSI/ESDA/JEDEC JS-001-2017
CDM	C3	≥ 1000 V	JESD22-C101F

ESD HANDLING PRECAUTION: This device is designed to be Class 1A for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage

14. Tested in 5x5mm 32-Lead QFN-Style Package.

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FUNCTIONAL DIAGRAM

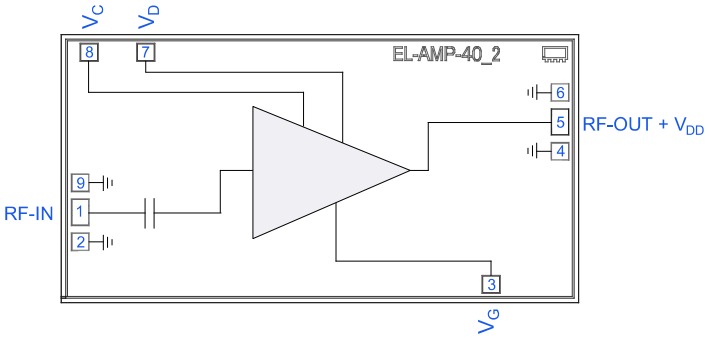

Figure 1. PVGA-273-D+ Functional Diagram

PAD DESCRIPTION[15]

Function	Pad Number	Application Description (Refer to Figure 3)
RF-IN	1	RF-IN Pad connects to the RF input port.
RF-OUT + V_{DD}	5	RF-OUT + V_{DD} Pad connects to RF output and drain voltage input port.
V_G	3	DC Input Pad connects to gate voltage input port.
V_D	7	DC Input Pad connects to drain voltage input port.
V_C	8	DC Input Pad connects to the control voltage input port.
GND	2,4,6 & 9	Connects to die backside through vias. bond wires to the ground are optional.

15. V_D and V_{DD} are separate independent voltage pins. PVGA-273-D+ can be operated by either applying +5 V (typ.) to Pad 5 RF-OUT + V_{DD} or +8 V (typ.) to Pad 7 V_D. Do not apply voltage to both Pad 5 and Pad 7 simultaneously. Applying voltage to both Pad 5 and Pad 7 simultaneously will damage the device.

DIE OUTLINE: inches [mm], Typical

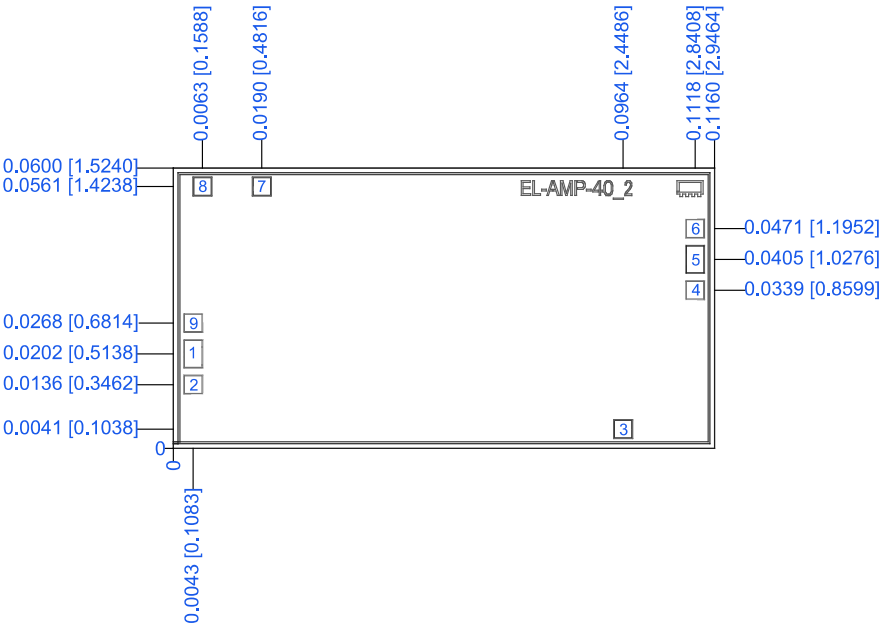

Figure 2. PVGA-273-D+ Die Outline

DIMENSIONS: inches [mm], Typical

Die Size	0.0600 x 0.1160 [1.5240 x 2.9464]
Die Thickness	0.0039 [0.1000]
Bond Pad Sizes:	
Pad 1 & 5	0.0059 x 0.0039 [0.1500 x 0.1000]
Pads 2-4, 6-9	0.0039 x 0.0039 [0.1000 x 0.1000]
Plating (Pads & Bottom of Die)	Gold

Variable Gain Amplifier PVGA-273-D+

50Ω 0.3 to 26.5 GHz High Dynamic Range

CHARACTERIZATION BOARD

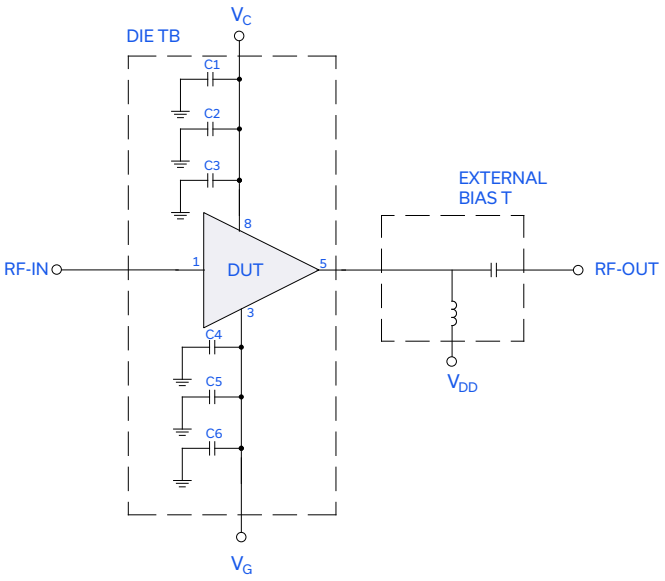

Figure 3. PVGA-273-D+ Characterization and Application Circuit.

Electrical Parameters and Conditions
Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3), and Noise Figure measured using N5247B PNA-X microwave network analyzer.

Conditions:
1. Gain and Return Loss: P_{IN} = -25 dBm.
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart:
   a. 0 dBm/Tone at Output when V_C = open.
   b. -9 dBm/Tone at Output when V_C is varied.

Caution: Permanent damage to the device will occur if the Power ON and Power OFF sequences are not followed.

Power ON:
1) Set V_G = -2 V. Apply V_G.
2) Set V_{DD} = +5 V. Apply V_{DD}.
3) Increase V_G to obtain the desired I_{DD} as shown in the Electrical Specification Table.
4) Apply V_C if required for variable gain control. Not required for typical operation.
5) Apply RF signal.

Power OFF:
1) Turn Off RF signal.
2) Turn Off V_C if applied.
3) Adjust V_G down to -2 V.
4) Turn Off V_{DD}.
5) Turn Off V_G.

Component	Value	Size	Part Number	Manufacturer
C1, C6	0.01 uF	0402	KGM05AR71H103KH	AVX Corporation
C2, C5	1 uF	0402	GRM155R61H105KE05D	Murata
C3, C4	100 pF	22 x 22 mil	MA4M3100	MACOM

Variable Gain Amplifier PVGA-273-D+

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ASSEMBLY DIAGRAM

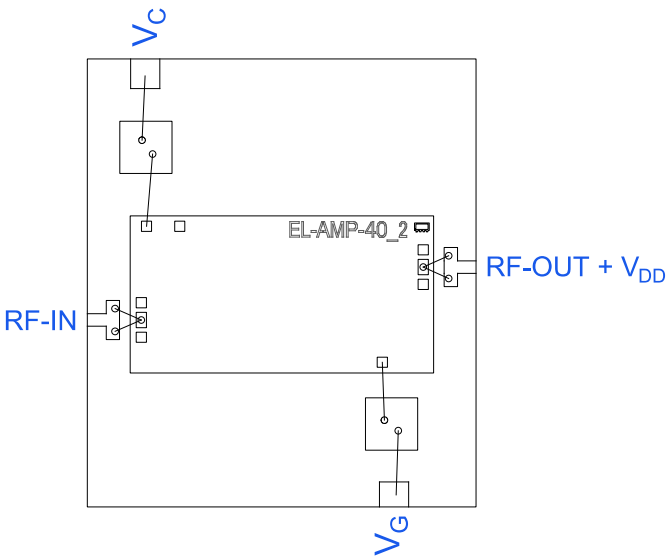

Figure 4. PVGA-273-D+ Assembly Diagram.

Refer to the table in Figure 3 for more details on the passive components.

- Bond wire diameter: 1 mil
- Bond wire lengths from Die Pad to PCB at
  - RF-IN & RF-OUT ports: 15 mils
  - V_G port: 30 mils
  - V_C port: 30 mils
- Typical Gap from Die edge to PCB edge: 2 mils
- PCB thickness and material: 8 mil Rogers RO4003C (Thickness: 1 oz copper on each side)

ASSEMBLY AND HANDLING PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccator or equivalent.
2. ESD Precautions
   MMIC pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices require careful handling using tools appropriate for manipulating semiconductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The surface of the chips have exposed air bridges and should not be touched with a vacuum collet, tweezers or fingers.
   The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is Ablestik 84-1 LMISR4 or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding
   Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire. Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance.

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ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASH BOARD CLICK HERE

Performance Data & Graphs	Data Graphs S-Parameter (S2P Files) Data Set (.zip file)	
Case Style	Die	
RoHS Status	Compliant	
Die Ordering and Packaging Information	Quantity, Package	Model No.
	Gel-Pak: 5, 10, or 50 KGD*	PVGA-273-DG+
	Medium†, Partial wafer: KGD*<493	PVGA-273-DP+
	Full wafer†	PVGA-273-DF+
	†Available upon request contact sales representative. Refer to AN-60-067	
Die Marking	EL-AMP-40_2	
Environmental Ratings	ENV80	

* Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a high degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.