Engineering Development Model

Frequency Synthesizer

RSN-EDR10612

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability.
At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.

Please click "Back", and then click "Contact Us" for Applications support.

CASE STYLE : JG1228

ELECTRICAL SPECIFICATIONS, 50Ω, over -40°C to +85°C					
Parameter		**Min.**	**Typ.**	**Max.**	**Units**
Frequency		1380		1380	MHz
Step size			20000		kHz
Settling Time	**Within ±1kHz**		1.5		msec
Output Power		+4	+7	+11	dBm
Phase Noise					
	at 100 Hz offset		-96		dBc/Hz
	at 1 kHz offset		-104		dBc/Hz
	at 10 KHz offset		-105	-99	dBc/Hz
	at 100 KHz offset		-132	-126	dBc/Hz
	at 1000 kHz offset		-153	-147	dBc/Hz
Integrated SSB Phase Noise			-61		dBc
Reference Spurious Suppression			-92		dBc
Comparison Spurious Suppression			-38		dBc
Non-Harm. Spurious Suppression			-90		dBc
Harmonic Suppression			-34	-28	dBc
Supply voltage	**VCO**		5		V
	PLL		3.3		V
Supply current	**VCO**		47	55	V
	PLL		21	29	V
(External) Reference In (External)	**Frequency**		960		MHz
	Amplitude		1		Vp-p
	Impedance		100		kΩ
	Ph. N @ 1kHz		-145		dBc/Hz
Digital Lock Detect	**Locked**	2.9		3.3	V
	Unlocked			0.4	
Frequency Synthesizer PLL		Self-programmed (internal microcontroller)			

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature	-45°C to 85°C
Storage Temperature	-55°C to 100°C
VCO Supply Voltage	6V
PLL Supply Voltage	4.3V
Reference Frequency voltage	3.6Vp-p

Power On sequence: Vcc VCO followed by Vcc PLL
Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS			
RF OUT	4	**N.C**	8,9,10,16,18
VCC VCO	19	**GROUND**	1,2,3,5,6,11, 13,14,15,20
VCC PLL	17		
REF IN	12		
LOCK DETECT	7		