

Ultra Low Noise, Medium Current  
**E-PHEMT Die**

**SAV-541-D+**

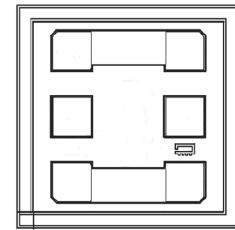
50Ω 0.45 to 6 GHz

**Product Features**

- Low Noise Figure, 0.4 dB
- Gain, 17 dB at 2 GHz
- High Output IP3, +33 dBm
- Output Power at 1dB comp., +21 dBm
- High Current, 15 to 60mA
- Wide bandwidth
- External biasing and matching required

**Typical Applications**

- Cellular
- ISM
- GSM
- WCDMA
- WiMax
- WLAN
- UNII and HIPERLAN



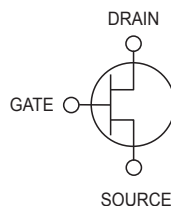
**+RoHS Compliant**  
 The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

*Ordering Information: Refer to Last Page*

**General Description**

SAV-541-D+ is an ultra-low noise, high IP3 transistor die, manufactured using E-PHEMT\* technology enabling it to work with a single positive supply voltage. It has outstanding Noise Figure, particularly below 2.5 GHz, and when combining this noise figure with high IP3 performance in a single device it makes it an ideal amplifier for demanding base station applications.

**Simplified Schematic and Pad description**



Pad	Description
Source	Ground
Gate	RF-IN
Drain	RF-OUT

\* Enhancement mode Pseudomorphic High Electron Mobility Transistor.

Note: 1. Bond Pad material - Gold  
 2. Bottom of Die - Gold plated

DC Electrical Specifications<sup>1</sup> at  $T_{AMB}=25^{\circ}\text{C}$ , Frequency 0.45 to 6 GHz

Symbol	Parameter	Condition	Typical			Units
$I_{DSS}$	Drain Current		15	30	60	mA
$V_{GS}$	Operational Gate Voltage	$V_{DS}=3\text{V}$ , at respective $I_{DS}$	0.34	0.39	0.48	V
$V_{TH}$	Threshold Voltage	$V_{DS}=3\text{V}$ , $I_{DS}=4\text{ mA}$	0.26	0.26	0.26	V
$I_{DSS}$	Saturated Drain Current	$V_{DS}=3\text{V}$ , $V_{GS}=0\text{ V}$	1.0	1.0	1.0	$\mu\text{A}$
$G_M$	Transconductance	$V_{DS}=3\text{V}$ , $G_m=\Delta I_{DS}/\Delta V_{GS}$ $\Delta V_{GS}=V_{GS1}-V_{GS2}$ $V_{GS1}=V_{GS}$ at respective $I_{DS}$ $V_{GS2}=V_{GS1}+0.05\text{V}$	251	327	392	mS

RF Electrical Specifications<sup>2</sup>

Symbol	Parameter	Condition (GHz)	$V_{DS}=3\text{V}$			$V_{DS}=4\text{V}$			Units
			$I_{DS}=15\text{mA}$	$I_{DS}=30\text{mA}$	$I_{DS}=60\text{mA}$	$I_{DS}=15\text{mA}$	$I_{DS}=30\text{mA}$	$I_{DS}=60\text{mA}$	
			Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	
$NF^2$	Noise Figure	0.9	0.34	0.28	0.25	0.35	0.27	0.25	dB
		2.0	0.46	0.35	0.33	0.5	0.34	0.38	
		3.9	0.66	0.62	0.53	0.63	0.52	0.53	
		5.8	1.50	1.18	1.40	1.47	1.29	1.36	
Gain	Gain	0.9	22.0	22.4	24.7	22.0	23.7	24.7	dB
		2.0	17.1	17.1	19.0	17.1	18.3	19.1	
		3.9	11.7	12.0	13.4	11.8	12.8	13.5	
		5.8	8.4	7.6	10.0	8.4	9.4	10.1	
OIP3	Output IP3	0.9	22.7	27.7	32.1	23.0	27.8	32.3	dBm
		2.0	21.7	27.4	32.9	22.1	27.7	33.1	
		3.9	23.9	30.2	32.6	24.4	30.0	35.7	
		5.8	22.0	28.3	33.8	22.5	28.3	35.8	
$P_{1dB^3}$	Power output at 1 dB Compression	0.9	16.9	17.3	18.5	20.0	18.5	20.6	dBm
		2.0	18.5	18.1	19.0	21.4	20.3	21.0	
		3.9	17.8	17.7	18.1	20.2	20.0	20.4	
		5.8	19.6	18.8	18.9	22.3	20.8	20.8	

1. Measured on industry standard SOT-343 (SC-70) package.

2. Measured on die using GSG (Ground-Signal-Ground) probe. See figure 1.

3. Drain current was allowed to increase during compression measurements.

Absolute Maximum Ratings<sup>4</sup>

Symbol	Parameter	Max.	Units
$V_{DS}^5$	Drain-Source Voltage	5	V
$V_{GS}^5$	Gate-Source Voltage	-5 to 0.7	V
$V_{GD}^5$	Gate-Drain Voltage	-5 to 0.7	V
$I_{DS}^5$	Drain Current	120	mA
$I_{GS}$	Gate Current	2	mA
$P_{DISS}$	Total Dissipated Power	360	mW
$P_{IN}^6$	RF Input Power	17	dBm
$T_{CH}$	Channel Temperature	150	$^{\circ}\text{C}$
$T_{OP}$	Operating Temperature	-40 to 85	$^{\circ}\text{C}$
$\Theta_{JC}$	Thermal Resistance	160	$^{\circ}\text{C}/\text{W}$

4. Operation of this device above any one of these parameters may cause permanent damage.

5. Assumes DC quiescent conditions.

6.  $I_{GS}$  is limited to 2 mA during test.

Characterization Test Circuit

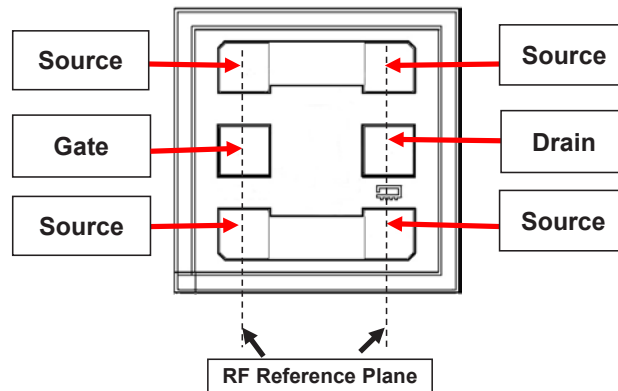


Fig 1. Block Diagram of Test Circuit used.

Gain, Return loss, Output Power at 1dB compression (P1dB), Output IP3 (OIP3) and Noise figure measured using Agilent's N5242A PNA-X Microwave network analyzer.

Conditions:

1. Drain voltage (with reference to source, VDS)=3 or 4V as shown.
2. Gain voltage (with reference to source, VGS) is set to obtain desired Drain-Source current (IDS) as shown.
3. Gain:Pin=-25 dBm
4. Output IP3 (OIP3)= two tones spaced 1 MHz apart. 0 dBm/tone at output.
5. No external matching components used.

Die Layout

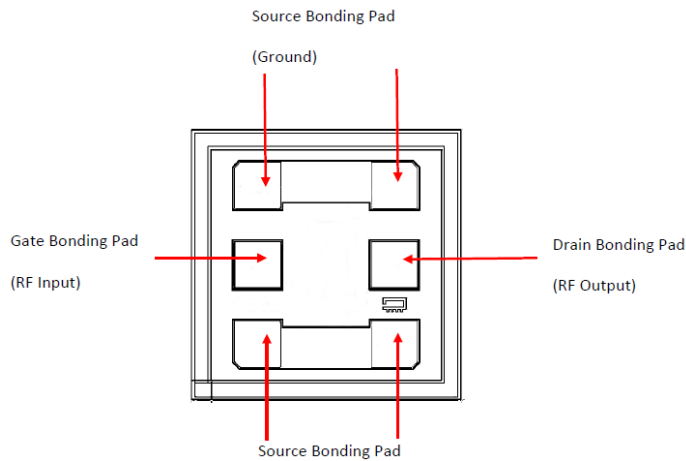


Fig 2. Die Layout

Bonding Pad Position  
(Dimensions in  $\mu\text{m}$ , Typical)

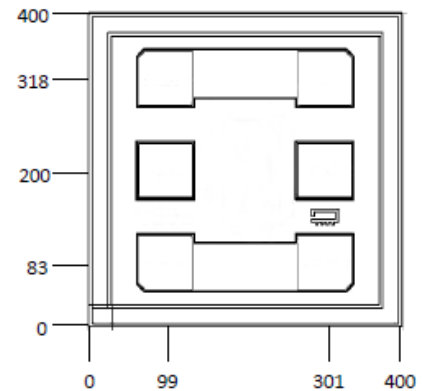


Fig 3. Bonding Pad Positions

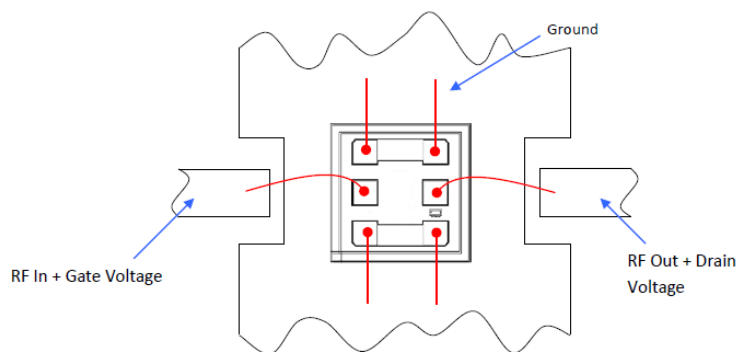
Critical Dimensions

Parameter	Values
Die Thickness, $\mu\text{m}$	100
Die Width, $\mu\text{m}$	400
Die Length, $\mu\text{m}$	400
Bond Pad Size, $\mu\text{m}$	75 x 75

## Assembly and Handling Procedure

1. Storage  
Dice should be stored in a dry nitrogen purged desiccators or equivalent.
2. ESD  
MMIC EPHEMPT amplifier dice are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be opened in clean room conditions at an appropriately grounded anti-static workstation. Devices need careful handling using correctly designed collets, vacuum pickup tips or sharp antistatic tweezers to deter ESD damage to dice.
3. Die Attach  
The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are DieMat DM6030HK-PT/H579 or Ablestik 84-1LMISR4. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total die periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. It is recommended to use antistatic die pick up tools only.
4. Wire Bonding  
Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the dice gold bond pads. Thermo-sonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1 mil diameter. Bonds must be made from the bond pads on the die to the package or substrate. All bond wires should be kept as short as low as reasonable to minimize performance degradation due to undesirable series inductance.

## Assembly Diagram



### Recommended Wire Length, Typical

Wire	Wire Length (mm)	Wire Loop Height (mm)
GATE, DRAIN	0.70	0.15
SOURCE (TO GROUND)	0.30	0.15

<b>Additional Detailed Technical Information</b> <i>additional information is available on our dash board.</i>	
<b>Performance Data</b>	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set with and without port extension(.zip file)
<b>Case Style</b>	Die
<b>Die Ordering and packaging information</b>	<p>Quantity, Package <span style="float: right;">Model No.</span></p> <p>Small, Gel - Pak: 10,50,100 KGD* <span style="float: right;">SAV-541-DG+</span></p> <p>Medium†, Partial wafer: KGD*&lt;3720 <span style="float: right;">SAV-541-DP+</span></p> <p>† Available upon request contact sales representative</p> <p>Refer to <a href="#">AN-60-067</a></p>
<b>Environmental Ratings</b>	ENV-80

## ESD Rating

Human Body Model (HBM): Class 1A (250 V to < 500 V) in accordance with ANSI/ESD STM 5.1 - 2001

\*\* Tested in industry standard 6-lead 400µmx400µm package.

### Additional Notes

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