Solid state

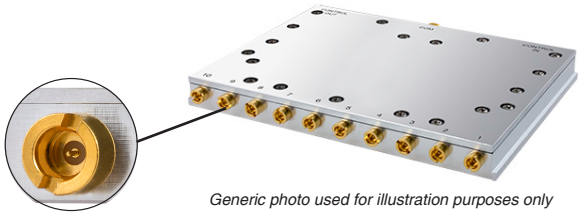
SPI RF SP10T Switch

SPI-SP10T-63

50Ω 1 to 6000 MHz

The Big Deal

- Daisy Chain SPI Control
- High Isolation (80 dB typ)
- High speed switching (6 µs typ)
- High power handling (+27 dBm max)
- SMP snap-on RF connectors



Generic photo used for illustration purposes only
Case Style: PM2137

Product Overview

Mini-Circuits' SPI-SP10T-63 is a low cost, high speed solid state RF SP10T absorptive switch, with control and power via a Digital Snap Fit connector. The model contains an electronic, high speed (6 µs typ switching time), high linearity (IP3 50 dBm typ), SP10T switch. The RF switch is operated using a 3-wire SPI interface compatible with TTL and LVTTL voltages and allows connecting up to 50 units in series to the same control line in a 'Daisy Chain' configuration. The RF switch operates over a wide frequency band from 1 to 6000 MHz with high isolation (80 dB typical) making the switch perfectly suitable for a wide variety of RF applications.

The SPI-SP10T-63 is constructed in a compact, rugged metal case (4.58" x 3.395" x 0.40") with 11 SMP(M) connectors (COM, and J1 to J10), and two Digital Snap-fit connectors providing a strong mechanical connection for SPI control and power, one for input and one for output when connecting multiple units in series.

Key Features

Feature	Advantages
Daisy chain SPI control	Allows connecting up to 50 units in series to a single power supply and 3 wire SPI control.
RF SP10T absorptive switch	Wideband (1 to 6000 MHz) with high isolation (80 dB typ.), and high power rating (+27 dBm through path).
High Linearity (IP3 +50 dBm typ.)	Results in little or negligible inter-modulation generation, meeting requirements for digital communications signals
Solid state switch	Provides high speed (6 µs typ) switching with no wear on the switch as with electro-mechanical designs
DC Blocking	No need for external DC blocking circuitry
SMP connectors	Snap on RF connectors allow quick assembly and disassembly and the small size of SMP connectors makes tighter assemblies possible

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Features

- High speed switching (6 µs typ)
- 1 to 6000 MHz SP10T absorptive RF switch
- High power handling, +27 dBm
- High linearity (IP3 +50 dBm)
- High isolation (80 dB typ)
- SPI control
- Daisy-chain up to 50 switches to control through a single interface (see pages 4-5)
- Easy installation and operation

Generic photo used for illustration purposes only

Case Style: PM2137

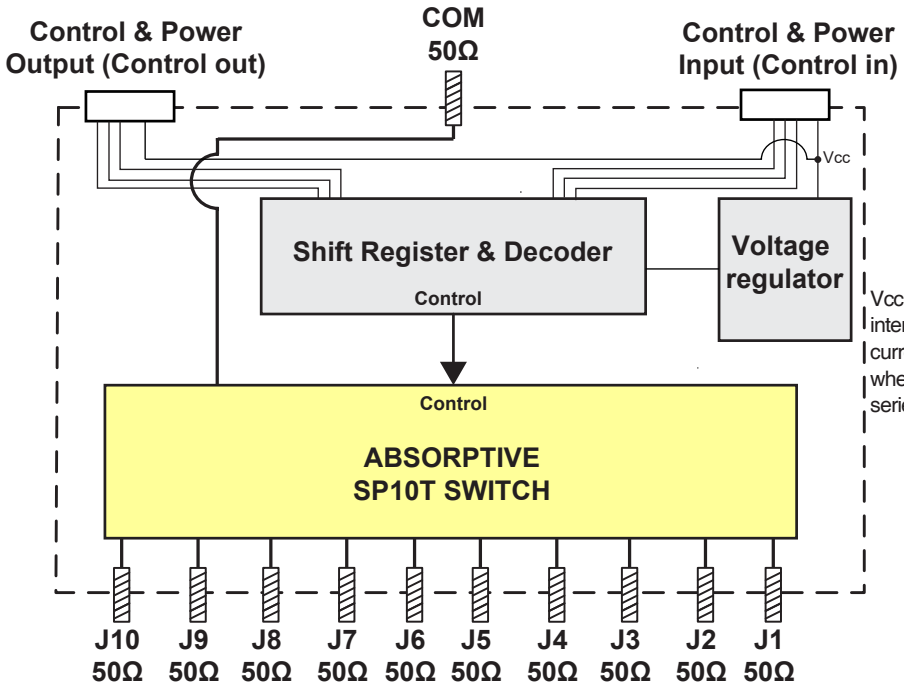
Applications

- R&D
- Automated Test equipment
- Controlling RF signal paths

RoHS Compliant

See our web site for RoHS Compliance methodologies and qualifications

Block Diagram



Vcc pins#1-3 and GND pins#4-6 are internally shorted to allow spreading current load between multiple lines when many units are connected in series.

RF Electrical Specifications @ +25°C

Parameter	Port	Conditions	Min.	Typ.	Max.	Units
Operating Frequency			1		6000	MHz
Insertion Loss	COM to active ports 1-4 or 7-10	1 to 3000 MHz	–	3.2	5.0	dB
		3000 to 6000 MHz	–	4.7	6.5	
	COM to active port 5, or 6	1 to 3000 MHz	–	2.1	4.0	
		3000 to 6000 MHz	–	3.2	5.0	
Isolation	Between any two ports of J1 to J10	1 to 3000 MHz	70	95	–	dB
		3000 to 6000 MHz	65	90	–	
	COM to any terminated port	1 to 3000 MHz	65	90	–	
		3000 to 6000 MHz	60	85	–	
VSWR	COM port	1 to 3000 MHz	–	1.25	–	:1
		3000 to 6000 MHz	–	1.40	–	
	Any port connected to COM	1 to 3000 MHz	–	1.25	–	
		3000 to 6000 MHz	–	1.45	–	
	Any terminated port	1 to 3000 MHz	–	1.10	–	
		3000 to 6000 MHz	–	1.25	–	
Power Input @1 dB Compression [1,2]	COM to any active port	1 to 6000 MHz	30	–	–	dBm
IP3 [3]	COM to any active port	10 to 6000 MHz	–	50	–	dBm
Switching time [4]	–	1 to 6000 MHz	–	6	–	µs
Operating RF Input Power	COM to any active port	Hot Switching	–	–	+17	dBm
	Any terminated port	–	–	–	+17	
	COM to any active port	Through path [1]	–	–	+27	
Control	Control is via SPI in at Control In port. Control Out can be used to connect multiple units in a 'Daisy chain' without additional controls					

[1] Max operating power degrades linearly below 10 MHz to +22 dBm at 1 MHz.
[2] Note absolute maximum ratings in table below
[3] Tested with 1 MHz span between signals, +5 dBm per tone.
[4] Tested between Trigger and 90% RF signal at RF port

Connections

RF Switch (J1 to J10, COM)	(SMP male)
Power & Control in (Control in)*	(Hirose ST 10 pin Connector) [5]
Power & Control out (Control out)**	(Hirose ST 10 pin Connector) [5]

[5] Mating connector is Hirose ST40X-10S-CV(30)

* Control in Pin Connections

Pin Number	Function
1 - 3	Vcc In
4 - 6	GND
7	Data In
8	Clock In
9	LE In
10	Lock in

** Control out Pin Connections

Pin Number	Function
1 - 3	Vcc out
4 - 6	GND
7	Data Out
8	Clock Out
9	LE Out
10	Lock Out

Absolute Maximum Ratings

Operating Temperature	0°C to 50°C
Storage Temperature	-20°C to 60°C
DC supply voltage max.	26V
Max supply current per pin	800 mA
RF power @ into inactive (internal termination) port	+20 dBm
RF power @ 1 -10 MHz into COM or active port	+25 dBm
RF power @ 10 -6000 MHz into COM or active port	+30 dBm
DC voltage @ RF Ports	16V

Permanent damage may occur if any of these limits are exceeded. Operating in the range between operating power limits and absolute maximum ratings for extended periods of time may result in reduced life and reliability.

DC Electrical Specifications

Parameter		Min.	Typ.	Max.	Units
Vcc, Supply Voltage		12	—	24	V
Load on Vcc between In and Out ports		—	0.05	—	Ω
Icc, Supply Current	@24V	—	30	—	mA
	@12V	—	50	—	
Control Input Low		-0.3	—	+0.6	V
Control Input High		2.0	—	5.5	V
Control Current		—	400	—	µA

Control Interface

The SPI-SP10T-63 serial interface consists of 4 control bits per unit that select the desired switch state, as shown in Table 1: Switch Logic Table.

Table 1: Switch Logic Table

A0	A1	A2	A3	Switch State
1	0	1	0	Com<->J1
1	0	1	1	Com<->J2
1	0	0	1	Com<->J3
1	0	0	0	Com<->J4
1	1	N.C.	N.C.	Com<->J5
0	1	N.C.	N.C.	Com<->J6
0	0	1	0	Com<->J7
0	0	1	1	Com<->J8
0	0	0	1	Com<->J9
0	0	0	0	Com<->J10

The serial interface is a 4-bit serial in, parallel-out shift register buffered by a transparent latch. It is controlled by three-wire SPI protocol using Data, Clock, and Latch Enable (LE) and an additional Lock for added noise immunity and increased flexibility in controlling the units. All signal voltages are compatible with TTL and LVTTL. The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input.

The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the switch. When LE is brought LOW, data in the shift register is latched.

Lock is used to lock the current state of the switch regardless of LE state or shift register, while allowing the LE to pass to other switches in the chain. If Lock is at logic HIGH the switch will respond to LE normally, when Lock is at logic LOW the switch will not respond to LE. If Lock is not required it can be kept constantly at logic high.

The shift register should be loaded while LE is held LOW to prevent the switch state from changing as data is entered. If multiple units are connected in series, data for all units should be entered before raising the LE to prevent switches assuming unanticipated states. Thus for example if three units are connected in daisy chain all 12 bits of control should be entered before raising the LE (see figures 2-4 for connecting units in daisy chain).

The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by Figure 1: Serial Interface Timing Diagram and Table 2: Serial Interface AC Characteristics.

Note:

1. LE is connected in parallel to all units in a daisy chain using the switches internal buffers to prevent control current from increasing as more units are connected.

Figure 1: Serial Interface Timing Diagram

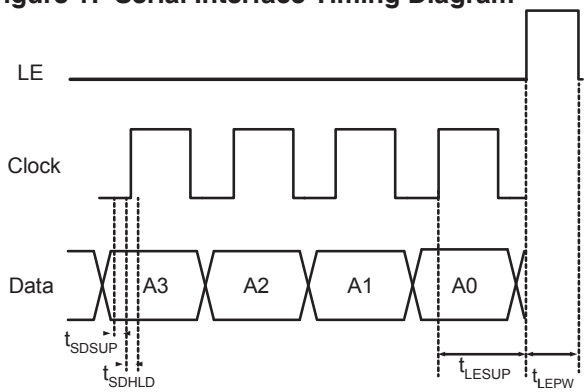


Table 2. Serial Interface AC Characteristics

Symbol	Parameter	Min.	Max.	Units
f_{clk}	Serial data clock frequency		20	MHz
t_{clkH}	Serial clock HIGH time	8		ns
t_{clkL}	Serial clock LOW time	14		ns
t_{LESUP}	LE set-up time after last clock rising edge	8		ns
t_{LEPW}	LE minimum pulse width	8		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	8		ns
t_{SDHLD}	Serial data hold time after clock falling edge	1		ns

Control Interface (Daisy Chain)

Figure 2: Connection diagram for multiple units in series

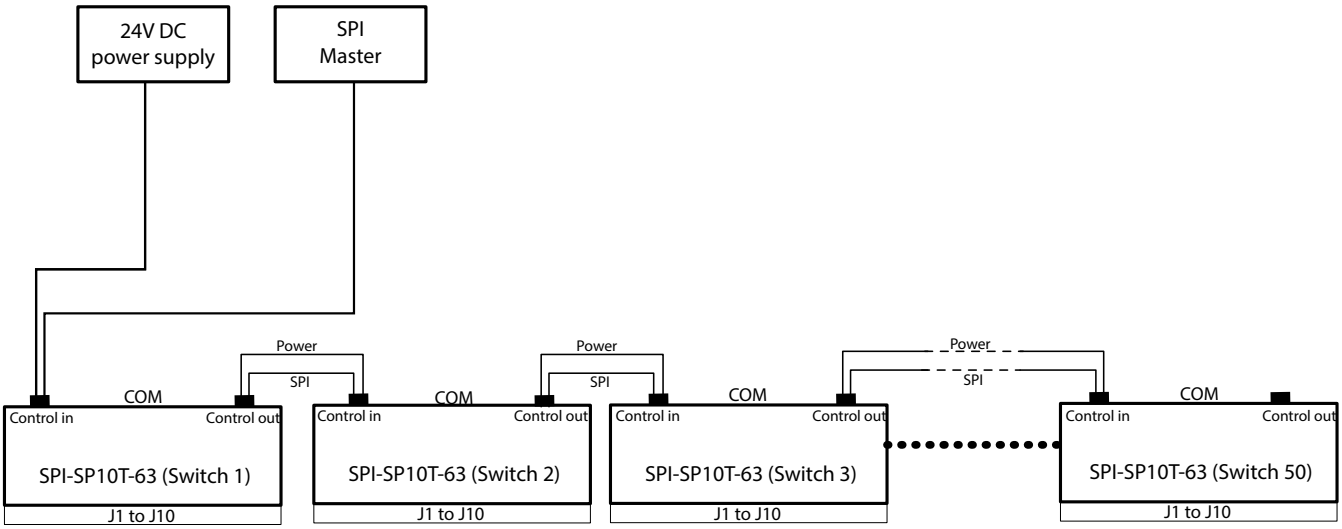


Figure 3: Serial Interface Timing Diagram for 3 units in series

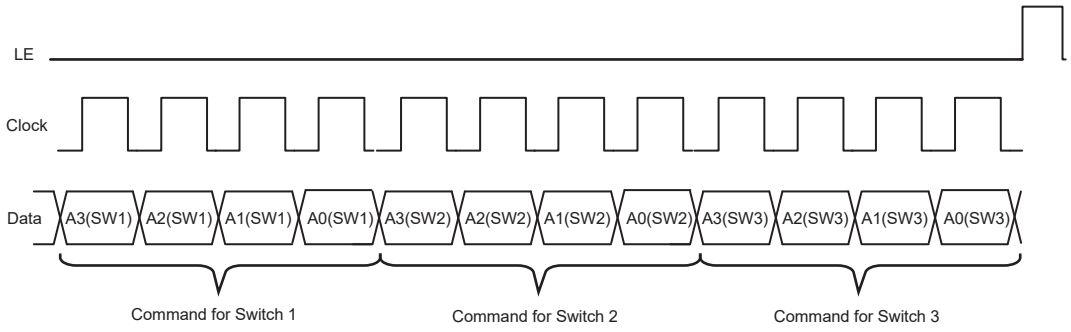
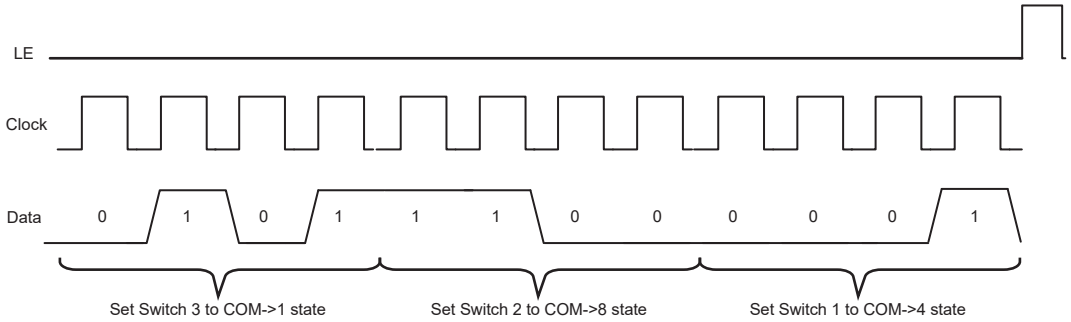
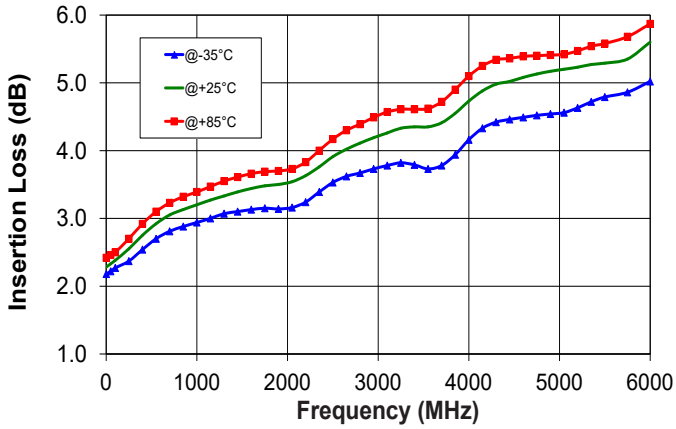


Figure 4: Example of command for 3 switches in series

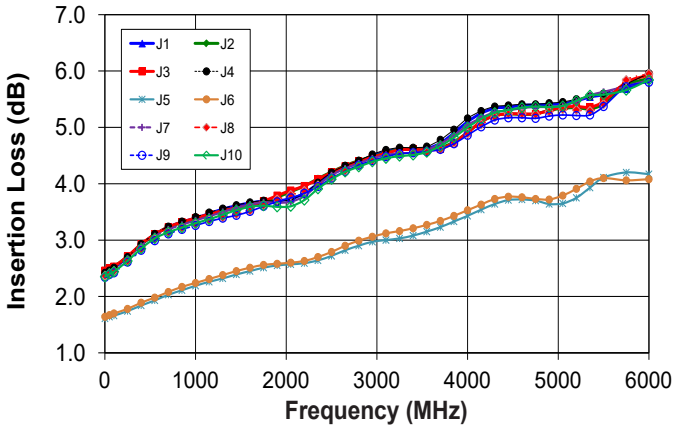


Typical Performance Curves

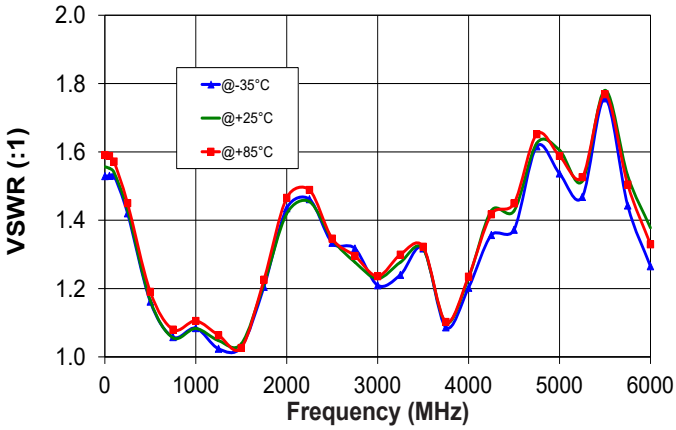
Insertion Loss over Temperature



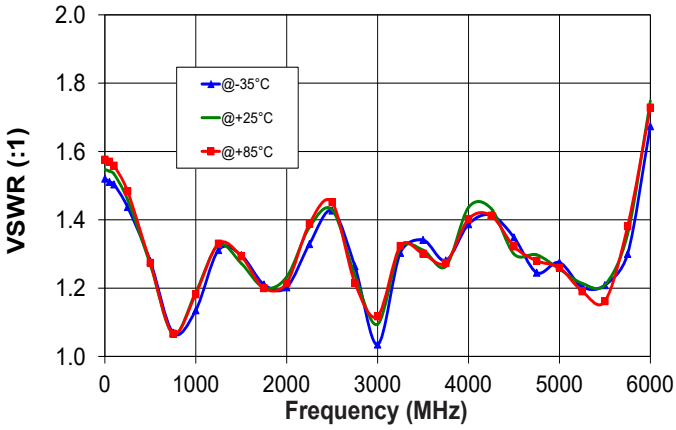
Insertion Loss at Ports J1-J10 vs. Frequency



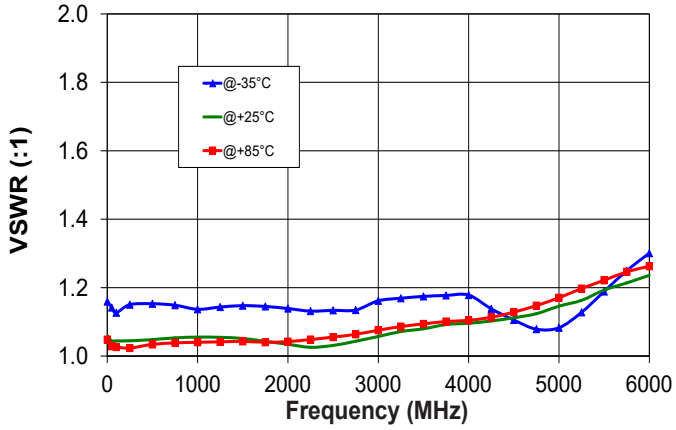
Active Port VSWR over Temp.



Common Port VSWR over Temp.

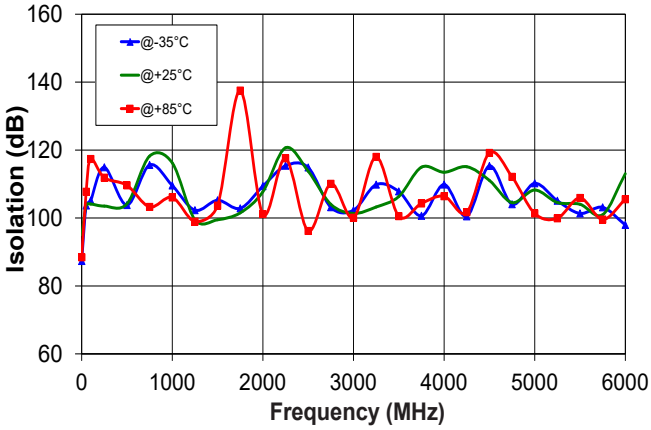


Internal Term. VSWR over Temp.

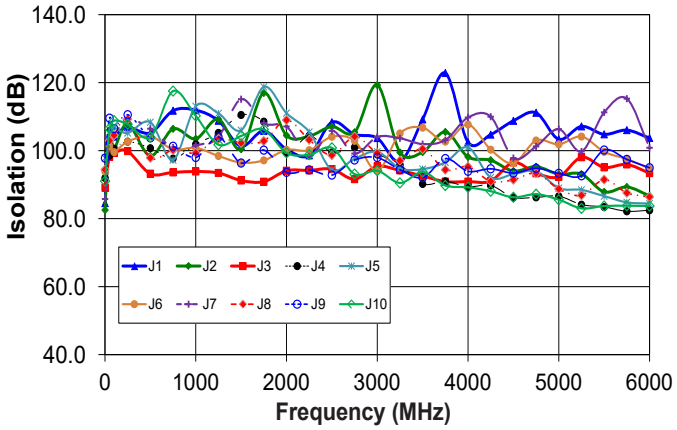


Typical Performance Curves (Continued)

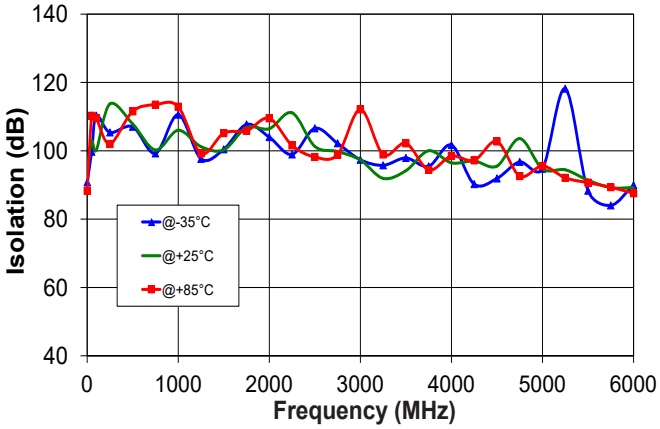
Isolation Com to Port 1 with Over temp.



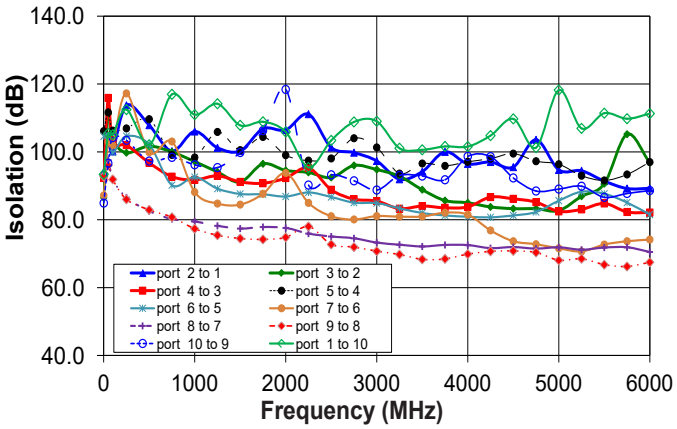
Isolation Com to Port J1-J10 vs. Frequency



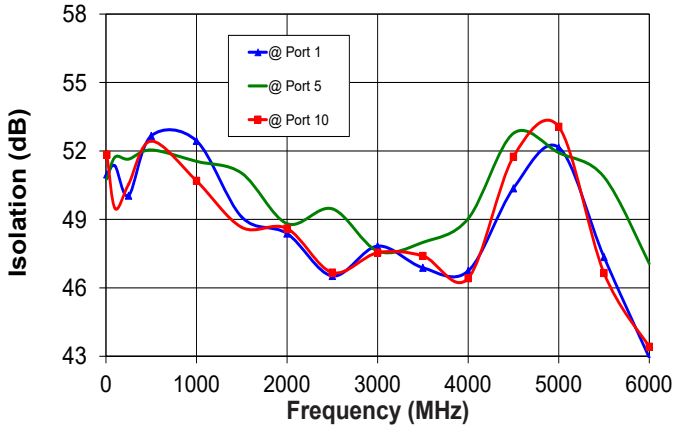
Isolation Port 2 to Port 1 Isolation over temp.



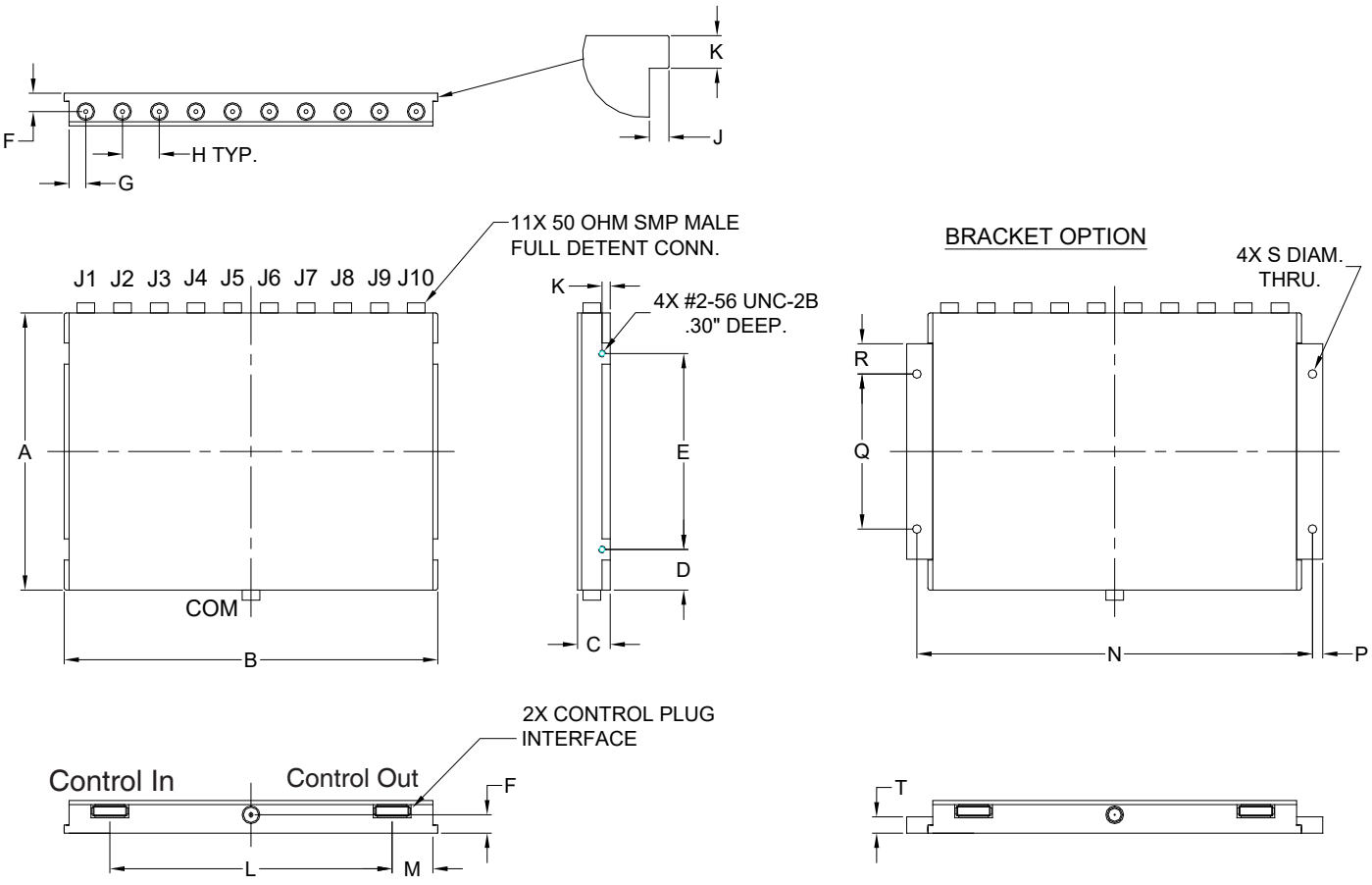
Isolation Port to Port vs. Frequency



Input IP3



Outline Drawing (PM2137)



Outline Dimensions (inch / mm)

A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	WT. GRAMS
3.395	**4.580**	**0.40**	**0.497**	**2.400**	**0.225**	**0.205**	**0.45**	**.060**	**0.100**	**3.460**	**0.500**	**4.850**	**0.125**	**1.900**	**0.370**	**0.106**	**0.200**	200
86.23	116.33	10.16	12.64	60.96	5.72	5.21	11.4	1.52	2.54	87.88	12.70	123.19	3.18	48.26	9.40	2.69	5.08	

Recommended Accessories

Several optional cable accessories with and without interface connector are available with the SPI-SP10T-63 in different lengths.

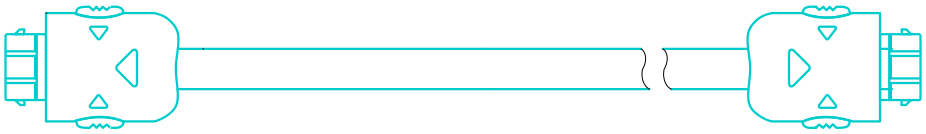
Cable P/N	Cable Length	Wire Gauge	Cable connectors	Recomended use
CBL-5FT-MMD+	5 ft (1.5 m)	32 AWG	Hirose ST40X-10S-CV(30) on each end	Connect between switches in series
CBL-1.5FT-MMD+	1.5 ft (0.46 m)	32 AWG	Hirose ST40X-10S-CV(30) on each end	Connect between switches in series
CBL-5FT-MPD+	5 ft (1.5 m)	32 AWG	Hirose ST40X-10S-CV(30) on one end, pigtail (bare wires) on the other	Connect SPI-SP10T-63 switch to customer control board and power

All cables are shielded and can handle the power draw of up to 50 switches in series.

CBL-5FT-MPD+ Control Cable

Pin Number	Function	Description	Pigtail Wire Color
1	Vcc	Supply Voltage	GREEN
2	Vcc	Supply Voltage	GREEN/BLACK
3	Vcc	Supply Voltage	RED
4	GND	Ground connection	ORANGE
5	GND	Ground connection	ORANGE/BLACK
6	GND	Ground connection	BLACK
7	Data	Data for SPI	RED/BLACK
8	Clock	Clock for SPI	BLUE
9	LE	Latch Enable for SPI	WHITE
10	Lock	Lock for SPI	WHITE/BLACK

CBL-5FT-MMD+ Control Cable



J1 Pin Number	J2 Pin Number	Function	Description
1	1	Vcc	Supply Voltage
2	2	Vcc	Supply Voltage
3	3	Vcc	Supply Voltage
4	4	GND	Ground connection
5	5	GND	Ground connection
6	6	GND	Ground connection
7	7	Data	Data for SPI
8	8	Clock	Clock for SPI
9	9	LE	Latch Enable for SPI
10	10	Lock	Lock for SPI

Ordering, Pricing & Availability Information see our web site

Model	Description
SPI-SP10T-63	SPI RF SP10T Switch

Optional Accessories	Description
CBL-5FT-MMD+	5 ft. Digital Snap Fit(male-male) cable assembly(SPI)
CBL-5FT-MPD+	5 ft. Digital Snap Fit(male-pigtail) cable assembly(SPI)
CBL-1.5FT-MMD+	1.5 ft. Digital Snap Fit(male-male) cable assembly(SPI)

Additional Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.

C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at www.minicircuits.com/MCLStore/terms.jsp