Engineering Development Model

Frequency Synthesizer

SSN-EDR11130SA

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



Please click "Back", and then click "Contact Us" for Applications support.

CASE STYLE: KJ1367

ELECTRICAL SPECIFICATIONS 50Ω, over -10°C to +75°C						
Parameter	Min.	Тур.	Max.	Units		
Frequency	1200		1400	MHz		
Step size		500		kHz		
Settling Time Within ±1kHz		0.9		msec		
Output Power	+1	+5	+10	dBm		
Phase Noise at 100 Hz offs at 1 kHz offs	set	-90 -93		dBc/Hz dBc/Hz		
at 10 KHz offs at 100 KHz offs at 1000 kHz offs	set	-92 -92 -133	-127	dBc/Hz dBc/Hz dBc/Hz		
Integrated SSB Phase Noise		-39		dBc		
Reference Spurious Suppression		-81		dBc		
Comparison Spurious Suppression		-109		dBc		
Non-Harm. Spurious Suppression	0 1	-90		dBc		
Harmonic Suppression		-37	-28	dBc		
Supply voltage VCO PLL		5 3. 3		V V		
Supply current VCO PLL	40	45 10	53 18	mA mA		
Frequency Reference In Amplitude (External) Impedance Ph. N @ 1kHz		10 1 100 -145		MHz Vp-p kΩ dBc/Hz		
Input Logic Logic high Levels Logic Low	2.64		3.3 0.66	V		
Digital Lock Locked Detect Unlocked	2.9		3.3 0.4	V		
Frequency Synthesizer PLL ADF4113						

ABSOLUTE MAXIMUM RATINGS				
Operating Temperature	-45°C to 85°C			
Storage Temperature	-55°C to 100°C			
VCO Supply Voltage	6V			
PLL Supply Voltage	4.3V			
Reference Frequency voltage	5.8Vp-p			
Data, Clock & LE levels	3.6V			

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS				
RF OUT	9	CLOCK	1	
VCC VCO	7	DATA	2	
VCC PLL	12	LATCH ENABLE	3	
REF IN	4	GROUND	5,6,8,10	
LOCK DETECT	11			