Engineering Development Model

Frequency Synthesizer

SSN-EDR11277SA

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



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CASE STYLE: KJ1367

ELECTRICAL SPECIFICATIONS 50Ω, over -15°C to +75°C						
Parameter		Min.	Тур.	Max.	Units	
Frequency		1380		1480	MHz	
Step size			100		kHz	
Settling Time W	/ithin ±1kHz		8.5		msec	
Output Power		-3	+1	+5	dBm	
Phase Noise						
	at 100 Hz offset		-89		dBc/Hz	
	at 1 kHz offset		-92		dBc/Hz	
	at 10 KHz offset		-100	-94	dBc/Hz	
	at 100 KHz offset		-125		dBc/Hz	
	at 1000 kHz offset		-146	-140	dBc/Hz	
Integrated SSB Phase Noise			-52		dBc	
Ref & Comp Spurious Suppression			-81		dBc	
0.5 Step size Spurious Suppression			-96		dBc	
Non-Harm. Spurious Suppression			-90		dBc	
Harmonic Suppression	1		-37		dBc	
Supply voltage	VCO		5		V	
Supply voltage	PLL		3.3		V	
Supply current	VCO		48	56	V	
	PLL		14	23	V	
	Frequency		10		MHz	
Reference In	Amplitude		1		Vp-p	
(External)	Impedance		100		kΩ	
	Ph. N @ 1kHz		-145		dBc/Hz	
Input Logic	Logic high	1.4		3.3	V	
Levels	Logic Low			0.6	V	
Digital Lock	Locked	1.4		3.3	V	
Detect	Unlocked			0.4	V	
Frequency Synthesizer PLL			ADF41	53		

ABSOLUTE MAXIMUM RATINGS				
Operating Temperature	-45°C to 85°C			
Storage Temperature	-55°C to 100°C			
VCO Supply Voltage	6V			
PLL Supply Voltage	4.3V			
Reference Frequency voltage	3.6Vp-p			
Data, Clock & LE levels	3.6V			

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS					
RF OUT	9	CLOCK	1		
VCC VCO	7	DATA	2		
VCC PLL	12	LATCH ENABLE	3		
REF IN	4	GROUND	5,6,8,10		
LOCK DETECT	11				