Engineering Development Model

Frequency Synthesizer

SSN-EDR9433/1

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability.
At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.

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CASE STYLE : 99-01-769

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C					
Parameter		**Min.**	**Typ.**	**Max.**	**Units**
Frequency		5900		6100	MHz
Step size			500		kHz
Settling Time	Within ±1kHz		3		msec
Output Power		-3	+2	+6	dBm
Phase Noise					
	at 100 Hz offset		-71		dBc/Hz
	at 1 kHz offset		-68		dBc/Hz
	at 10 KHz offset		-78		dBc/Hz
	at 100 KHz offset		-109	-103	dBc/Hz
	at 1000 kHz offset		-130		dBc/Hz
Integrated SSB Phase Noise			-30		dBc
Reference Spurious Suppression			-89		dBc
Comparison Spurious Suppression			-99		dBc
Non-Harm. Spurious Suppression			-90		dBc
Harmonic Suppression			-22		dBc
Supply voltage	VCO		5		V
	PLL		5		V
Supply current	VCO		67	76	mA
	PLL		9	17	mA
Reference In (External)	Frequency		10		MHz
	Amplitude		1		Vp-p
	Impedance		100		kΩ
	Ph. N @ 1kHz		-145		dBc/Hz
Input Logic Levels	Logic high	4		5	V
	Logic Low			1	
Digital Lock Detect	Locked	4.6		5	V
	Unlocked			0.4	
Frequency Synthesizer PLL		ADF4118			

ABSOLUTE MAXIMUM RATINGS	
Operating Temperature	-45°C to 85°C
Storage Temperature	-55°C to 100°C
VCO Supply Voltage	6V
PLL Supply Voltage	6V
Reference Frequency voltage	5.8Vp-p
Data, Clock & LE levels	5.3V

Power On sequence: Vcc VCO followed by Vcc PLL
Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS			
RF OUT	9	**CLOCK**	1
VCC VCO	7	**DATA**	2
VCC PLL	12	**LATCH ENABLE**	3
REF IN	4	**GROUND**	5,6,8,10
LOCK DETECT	11		