Engineering Development Model

Frequency Synthesizer

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



SSN-EDR9582

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CASE STYLE: KJ1367

ELECTRICAL SPECIFICATIONS 50Ω, over -40°C to +85°C							
Parameter		Min.	Тур.	Max.	Units		
Frequency		1542		1557	MHz		
Step size		70	200		kHz		
Settling Time Within ±1kHz			2		msec		
Output Power		0	+4	+7	₫₿m		
Phase Noise	at 100 Hz offset at 1 kHz offset		-90 -98		dBc/Hz dBc/Hz		
	at 10 KHz offset at 100 KHz offset at 1000 kHz offset		-101 -127 -148	-95 -122 -142	dBc/Hz dBc/Hz dBc/Hz		
Integrated SSB Phase Noise		440	-57		dBc		
Reference Spurious Suppression			-87	W (2)	dBc		
Comparison Spurious Suppression			-90		dBc		
0.5 Step size Spurious Suppression		200	-104		dBc		
Non-Harm. Spurious Suppression			-90		dBc		
Harmonic Suppression			-30	-21	dBc		
Supply voltage	VCO PLL		4.75 3.11		V V		
Supply current	VCO PLL	.10	47 16	55 25	V V		
	Frequency Amplitude		52 1		MHz Vp-p		
	mpedance n. N @ 1kHz		100 -145		kΩ dBc/Hz		
Input Logic	Logic high Logic Low	1.4		3.11 0.6	V		
Digital Lock Detect	Locked Unlocked	1.4		3.11 0.4	V		
Frequency Synthesizer PLL		ADF4153					

ABSOLUTE MAXIMUM RATINGS				
Operating Temperature	-45°C to 85°C			
Storage Temperature	-55°C to 100°C			
VCO Supply Voltage	5.75V			
PLL Supply Voltage	4.11V			
Reference Frequency voltage	3.6Vp-p			
Data, Clock & LE levels	3.41V			

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS					
RF OUT	9	CLOCK	1		
VCC VCO	7	DATA	2		
VCC PLL	12	LATCH ENABLE	3		
REF IN	4	GROUND	5,6,8,10		
LOCK DETECT	11				