## Engineering Development Model

## **Frequency Synthesizer**

## **Important Note**

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.

Please click "Back", and then click "Contact Us" for Applications support.

## TSN-EDR10938/1



**CASE STYLE: 99-01-1777** 

ELECTRICAL SPECIFICATIONS 50Ω, over -45°C to +85°C						
Parameter	Min.	Тур.	Max.	Units		
Frequency	1970		2250	MHz		
Step size		10000		kHz		
Settling Time Within ±1kHz		2.5		msec		
Output Power	+10	+14	+18	₽		
Phase Noise at 100 Hz offs at 1 kHz offs at 10 KHz offs at 100 KHz offs	et et et	-89 -98 -99 -121	-116	dBc/Hz dBc/Hz dBc/Hz dBc/Hz		
at 1000 kHz offs	et	-144	-138	dBc/Hz		
Integrated SSB Phase Noise	- AC	-53		dBc		
Ref & Comp Spurious Suppression		-102		dBc		
Non-Harm. Spurious Suppression		-90		dBc		
Harmonic Suppression		-33	-24	dBc		
Supply voltage VCO PLL		5 3		V V		
Supply current VCO PLL		59 11	68 19	mA mA		
Reference In (External)  Frequency Amplitude Impedance Ph. N @ 1kHz	400	10 1 100 -145		MHz Vp-p kΩ dBc/Hz		
Input Logic Logic high Levels Logic Low	1.4		3 0.6	V		
Digital Lock Detect Unlocked	2.6		3 0.4	V		
Frequency Synthesizer PLL ADF4106						

ABSOLUTE MAXIMUM RATINGS					
Operating Temperature	-45°C to 85°C				
Storage Temperature	-55°C to 100°C				
VCO Supply Voltage	6V				
PLL Supply Voltage	4V				
Reference Frequency voltage	3.6Vp-p				
Data, Clock & LE levels	3.3V				

Power On sequence: Vcc VCO followed by Vcc PLL Power Off sequence: Vcc PLL followed by Vcc VCO

PIN CONNECTIONS					
RF OUT	13	CLOCK	2		
VCC VCO	14	DATA	3		
VCC PLL	15	LOAD ENABLE	4		
REF IN	16	V-TUNE MONITOR	5		
LOCK DETECT	1	GROUND	6-12,17-22		