MMIC DIE

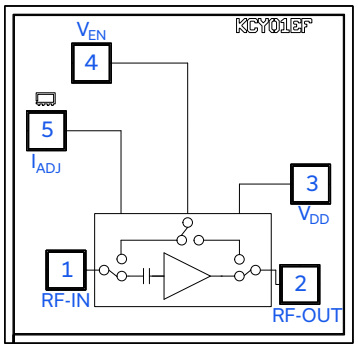
Low Noise Amplifier TSY-83LN-D+

50Ω 400 to 8000 MHz Bypass Mode Feature

THE BIG DEAL

- Low Loss Bypass Mode Feature
- Low Noise Figure, Typ. 1.4 dB
- High OIP3, Typ. +34.6 dBm
- High P1dB, Typ. +22.8 dBm

FUNCTIONAL DIAGRAM



SEE ORDERING INFORMATION ON THE LAST PAGE

APPLICATIONS

- Radar, EW, and ECM Defense Systems
- 5G Sub6, MIMO Wireless Infrastructure Systems
- Test & Measurement Equipment

PRODUCT OVERVIEW

Mini-Circuits' TSY-83LN-D+ is a GaAs pHEMT-based wideband, bypass mode-capable, low noise MMIC amplifier with a combination of high IP3 and flat gain. Operating from 400 to 8000 MHz, this amplifier features high dynamic range with 1.4 dB noise figure, 23 dB gain, +22.8 dBm P1dB, and +34.6 dBm OIP3. This combination of characteristics makes it ideal for sensitive, high dynamic range receiver applications where a gain stage may need to be quickly bypassed and shut down in the presence of high power RF signals. TSY-83LN-D+ operates on a single +5 V or +6 V supply and is well-matched to 50Ω.

KEY FEATURES

Features	Advantages
Bypass Mode Feature	Allows the user to quickly switch to a low loss bypass path while keeping the power supply at constant voltage to reduce gain and protect the system in the presence of high power RF signals while minimizing power consumption.
Low Noise Figure, Typ. 1.4 dB at 2000 MHz	Extremely low noise figure provides minimal signal-to-noise degradation in amplification mode.
High OIP3, Typ. +34.6 dBm at 2000 MHz	The combination of low noise figure and high IP3 makes this MMIC amplifier ideal for use in sensitive low noise receiver front ends where high dynamic range is of paramount importance.
Wide Bandwidth with Flat Gain: ±0.9 dB over 400 to 6000 MHz	Enables a single amplifier to be used across many applications including aerospace and defense (Radar, SATCOM, EW), broadband test instrumentation, telecommunications (5G Sub6), and more.
Unpackaged Die	Suitable for chip and wire hybrid assemblies.

REV. OR
ECO-026824
TSY-83LN-D+
MCL NY
250902

Low Noise Amplifier TSY-83LN-D+

50Ω 400 to 8000 MHz Bypass Mode Feature

ELECTRICAL SPECIFICATIONS[1] AT +25°C, V_{DD} = +6 V, AND Zo = 50Ω UNLESS NOTED OTHERWISE

Parameter	Condition (MHz)	Amplifier - ON			Amplifier - Bypass	Units
		Min.	Typ.	Max.	Typ.	
Frequency Range		400		8000	400-8000	MHz
Gain	400		22.2		-1.3	dB
	2000		22.8		-0.8	
	4000		23.0		-1.2	
	6000		24.0		-1.6	
	8000[2]		23.8		-3.0	
Input Return Loss	400		13		9	dB
	2000		18		17	
	4000		12		14	
	6000		20		9	
	8000[2]		8		6	
Output Return Loss	400		14		13	dB
	2000		20		17	
	4000		18		20	
	6000		20		10	
	8000[2]		12		6	
Isolation	400-8000		28.7			dB
Output Power at 1 dB Compression (P1dB)	400		+22.2		+12.2	dBm
	2000		+22.8		+13.3	
	4000		+22.1		+15.5	
	6000		+21.4		+15.6	
	8000[2]		+21.0		+15.5	
Output Third-Order Intercept Point (P_{OUT} = 0 dBm/Tone)	400		+37.2		+41.9	dBm
	2000		+34.6		+45.7	
	4000		+29.6		+45.0	
	6000		+28.2		+44.8	
	8000[2]		+26.5		+43.5	
Noise Figure	400		2			dB
	2000		1.4			
	4000		1.6			
	6000		1.7			
	8000[2]		1.7			
Device Operating Voltage (V_{DD})			+6		+6	V
Device Operating Current (I_{DD})[3]			104		4	mA
Enable Voltage (V_{EN})[4]			+6		0	V
Enable Current (I_{EN})			4.6		1.7	mA
Device Current Adjust (I_{ADJ})[5]			13		13	µA
Device Current Variation Vs. Temperature[6]			-57		-57	µA/°C
Device Current Variation Vs. Voltage[7]			0.028		0.028	mA/mV

1. Tested on Mini-Circuits Die Characterization 400-6000 MHz Test Board. See Figure 3. Board loss de-embedded.
2. Tested on Mini-Circuits Die Characterization 5500-8000 MHz Test Board. See Figure 4. Board loss de-embedded.
3. Current at P_{IN} = -25 dBm. Increases to 150 mA at P1dB.
4. V_{EN} must be equal to V_{DD} in Amplifier – ON mode.
5. I_{ADJ} is not intended as a voltage input port. Gain is nominal when I_{ADJ} is left open. When I_{ADJ} is open, there is a measured voltage of +1.4 V on the pin. To change the current, add a shunt resistor (see Figures 3 and 4).
6. (Current at +105°C - Current at -45°C) / (+150 °C).
7. (Current at +6 V - Current at +5 V) / (+6 V - +5 V).

Low Noise Amplifier TSY-83LN-D+

50Ω 400 to 8000 MHz Bypass Mode Feature

ELECTRICAL SPECIFICATIONS[8] AT +25°C, V_{DD} = +5 V, AND Zo = 50Ω UNLESS NOTED OTHERWISE

Parameter	Condition (MHz)	Amplifier - ON			Amplifier - Bypass	Units
		Min.	Typ.	Max.	Typ.	
Frequency Range		400		8000	400-8000	MHz
Gain	400		21.7		-1.3	dB
	2000		22.3		-0.9	
	4000		22.4		-1.2	
	6000		23.3		-1.6	
	8000[9]		23.1		-3.1	
Input Return Loss	400		12		9	dB
	2000		17		17	
	4000		11		14	
	6000		20		9	
	8000[9]		8		6	
Output Return Loss	400		14		13	dB
	2000		20		17	
	4000		16		20	
	6000		20		10	
	8000[9]		15		6	
Isolation	400-8000		28.4			dB
Output Power at 1 dB Compression (P1dB)	400		+20.1		+12.3	dBm
	2000		+21.0		+13.4	
	4000		+20.0		+15.6	
	6000		+19.3		+15.9	
	8000[9]		+19.3		+15.8	
Output Third-Order Intercept Point (P_{OUT} = 0 dBm/Tone)	400		+33.5		+42.4	dBm
	2000		+31.5		+45.9	
	4000		+27.6		+45.1	
	6000		+27.0		+44.6	
	8000[9]		+25.1		+43.7	
Noise Figure	400		1.9			dB
	2000		1.4			
	4000		1.5			
	6000		1.6			
	8000[9]		1.6			
Device Operating Voltage (V_{DD})			+5		+5	V
Device Operating Current (I_{DD})[10]			76		3	mA
Enable Voltage (V_{EN})[11]			+5		0	V
Enable Current (I_{EN})			4.5		1.7	mA
Device Current Adjust (I_{ADJ})[12]			13		13	µA
Device Current Variation Vs. Temperature[13]			-37		-37	µA/°C
Device Current Variation Vs. Voltage[14]			0.028		0.028	mA/mV

8. Tested on Mini-Circuits Die Characterization 400-6000 MHz Test Board. See Figure 3. Board loss de-embedded.
9. Tested on Mini-Circuits Die Characterization 5500-8000 MHz Test Board. See Figure 4. Board loss de-embedded.
10. Current at P_{IN} = -25 dBm. Increases to 140 mA at P1dB.
11. V_{EN} must be equal to V_{DD} in Amplifier – ON mode.
12. I_{ADJ} is not intended as a voltage input port. Gain is nominal when I_{ADJ} is left open. When I_{ADJ} is open, there is a measured voltage of +1.4 V on the pin. To change the current, add a shunt resistor (see Figures 3 and 4).
13. (Current at +105°C - Current at -45°C) / (+150 °C).
14. (Current at +6 V - Current at +5 V) / (+6 V - +5 V).

SWITCHING SPECIFICATIONS[15]

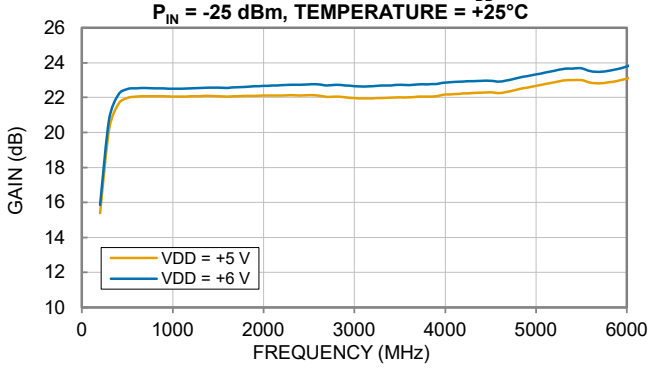
Parameter		+6 V Typ.	+5 V Typ.	Units
Amplifier ON to Bypass	OFF Time (50% Control to 10% RF)	16	17	ns
	FALL Time (90% to 10% RF)	17	17	ns
Amplifier Bypass to ON	ON Time (50% Control to 90% RF)	168	168	ns
	RISE Time (10% to 90% RF)	112	112	ns
Control Voltage Leakage		+97	+83	mV

15. Tested on packaged model TSY-83LN+ mounted on Mini-Circuits Characterization Test Board TB-TSY-83LNC+ (see TSY-83LN+ Datasheet for details).

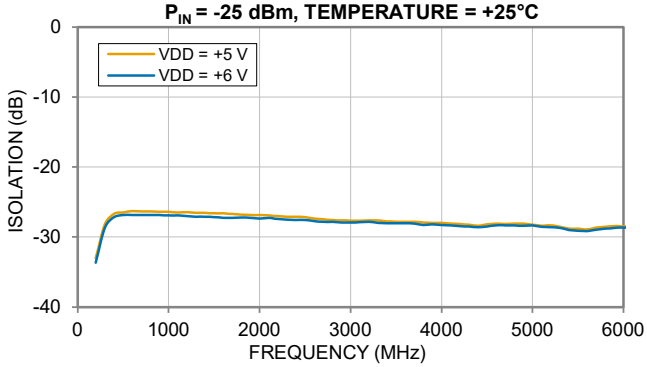
TYPICAL PERFORMANCE GRAPHS IN AMPLIFIER-ON MODE

Note: The following data was taken on the Mini-Circuits Die Characterization 400-6000 MHz Test Board (Figure 3). All data taken at nominal conditions V_{EN} = V_{DD} and RI_{ADJ} = Open unless noted otherwise. For additional over temperature graphs, see TSY-83LN+.

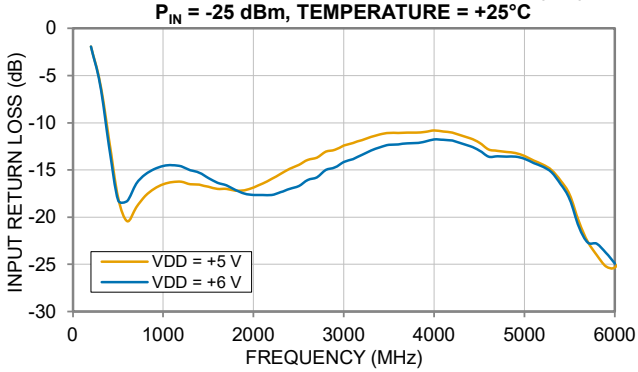
GAIN vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



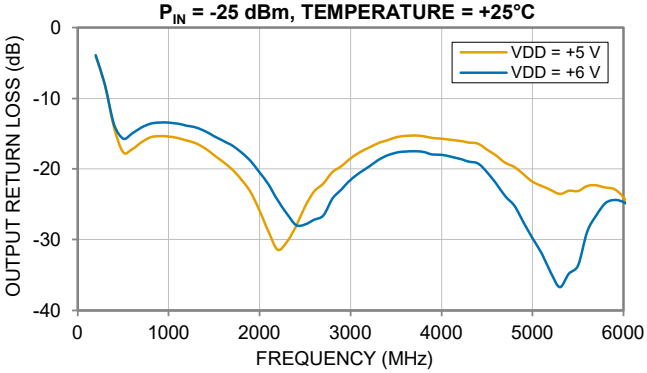
ISOLATION vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



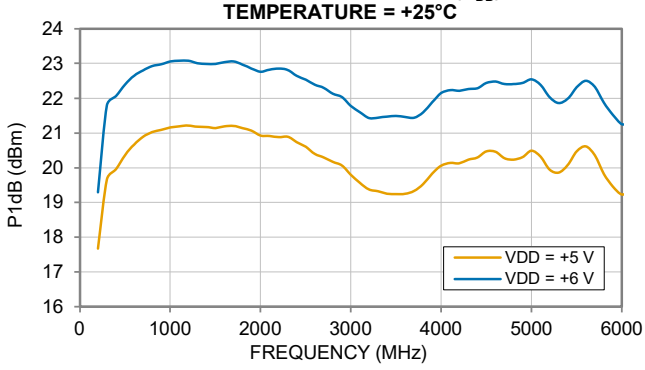
INPUT RETURN LOSS vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



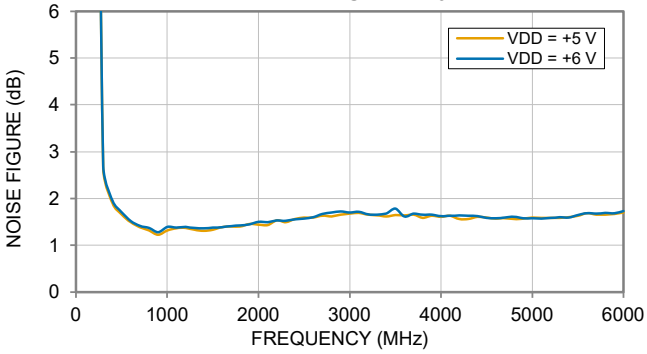
OUTPUT RETURN LOSS vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



P1dB vs. DEVICE VOLTAGE (V_{DD})
TEMPERATURE = +25°C



NOISE FIGURE vs. DEVICE VOLTAGE (V_{DD})
TEMPERATURE = +25°C



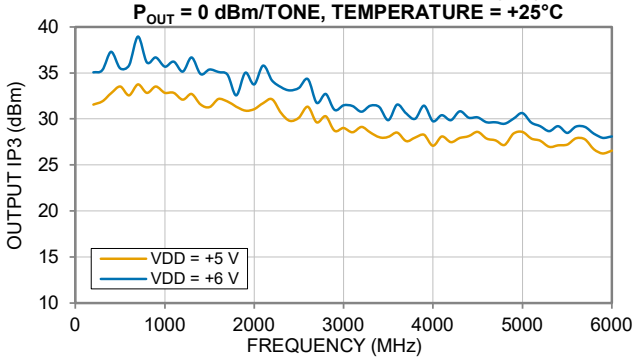
Low Noise Amplifier TSY-83LN-D+

50Ω 400 to 8000 MHz Bypass Mode Feature

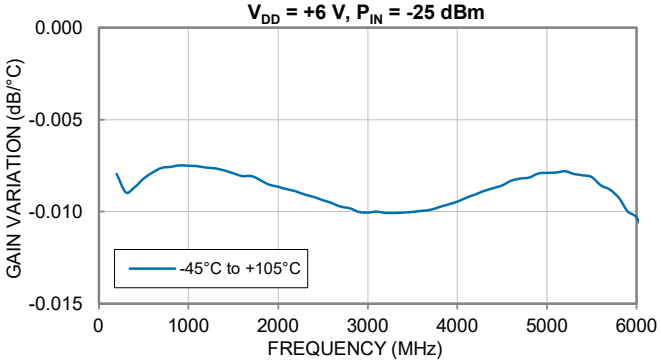
TYPICAL PERFORMANCE GRAPHS IN AMPLIFIER-ON MODE

Note: The following data was taken on the Mini-Circuits Die Characterization 400-6000 MHz Test Board (Figure 3). All data taken at nominal conditions V_{EN} = V_{DD} and RI_{ADJ} = Open unless noted otherwise. For additional graphs over temperature, see TSY-83LN+.

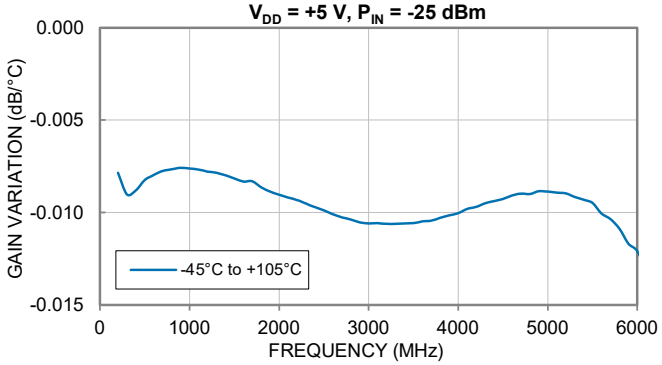
OUTPUT IP3 vs. DEVICE VOLTAGE (V_{DD})
P_{OUT} = 0 dBm/TONE, TEMPERATURE = +25°C



GAIN VARIATION vs. TEMPERATURE
V_{DD} = +6 V, P_{IN} = -25 dBm



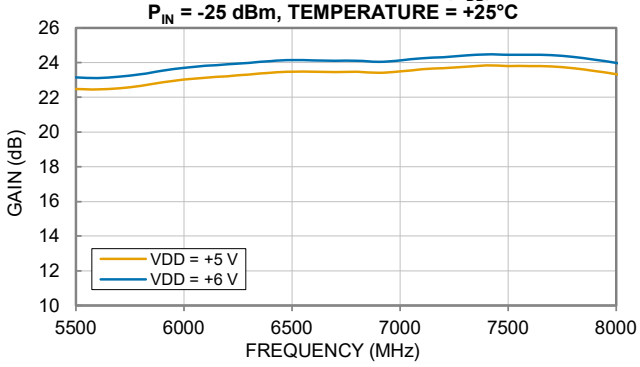
GAIN VARIATION vs. TEMPERATURE
V_{DD} = +5 V, P_{IN} = -25 dBm



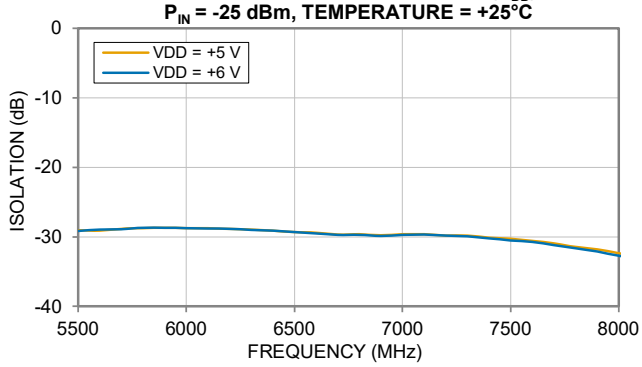
TYPICAL PERFORMANCE GRAPHS IN AMPLIFIER-ON MODE

Note: The following data was taken on the Mini-Circuits Die Characterization 5500-8000 MHz Test Board (Figure 4). All data taken at nominal conditions $V_{EN} = V_{DD}$ and RI_{ADJ} = Open unless noted otherwise. For additional graphs over temperature, see TSY-83LN+.

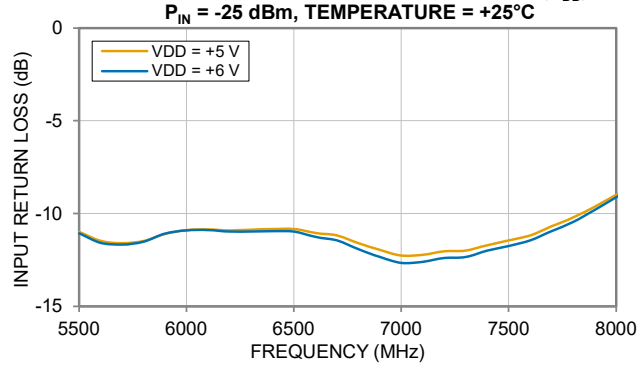
GAIN vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



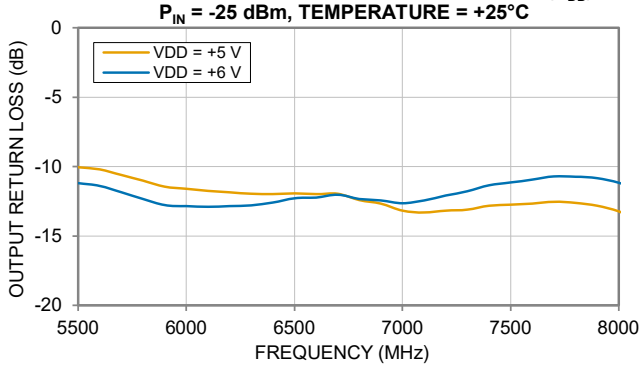
ISOLATION vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



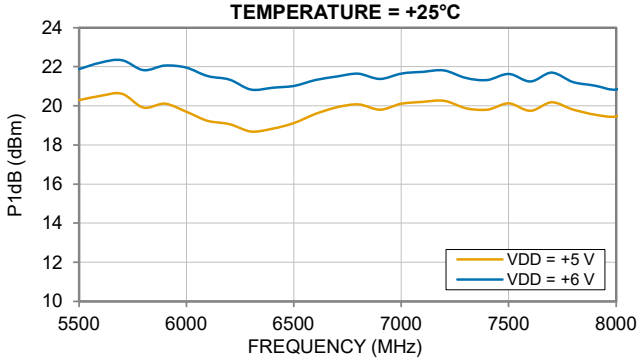
INPUT RETURN LOSS vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



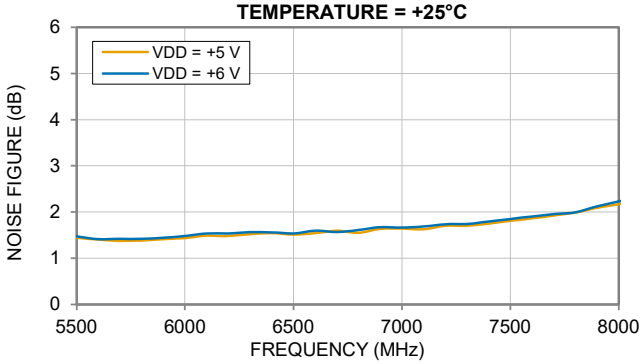
OUTPUT RETURN LOSS vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



P1dB vs. DEVICE VOLTAGE (V_{DD})
TEMPERATURE = +25°C



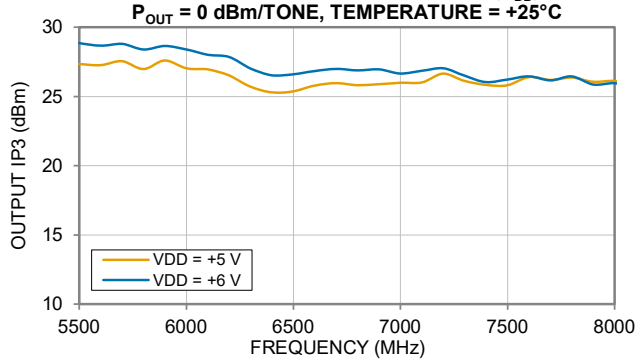
NOISE FIGURE vs. DEVICE VOLTAGE (V_{DD})
TEMPERATURE = +25°C



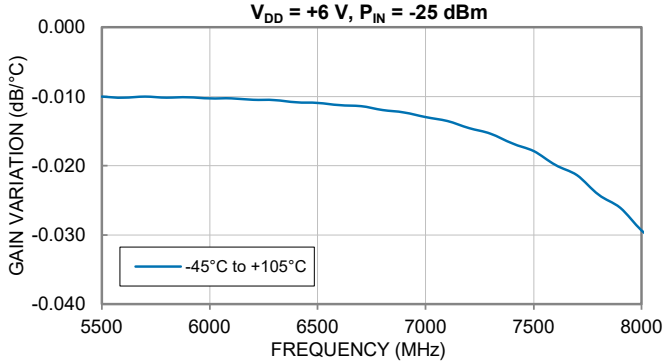
TYPICAL PERFORMANCE GRAPHS IN AMPLIFIER-ON MODE

Note: The following data was taken on the Mini-Circuits Die Characterization 5500-8000 MHz Test Board (Figure 4). All data taken at nominal conditions V_{EN} = V_{DD} and RI_{ADJ} = Open unless noted otherwise. For additional graphs over temperature, see TSY-83LN+.

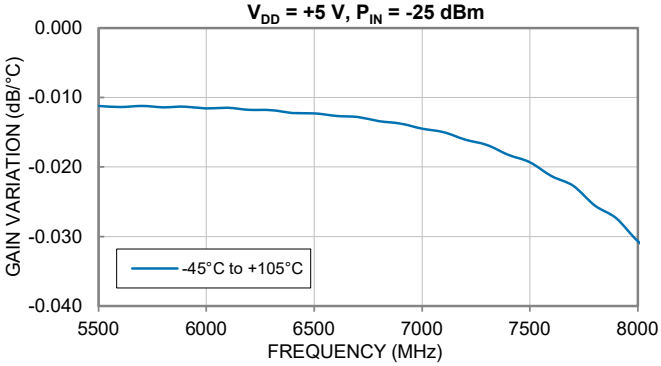
OUTPUT IP3 vs. DEVICE VOLTAGE (V_{DD})
P_{OUT} = 0 dBm/TONE, TEMPERATURE = +25°C



GAIN VARIATION vs. TEMPERATURE
V_{DD} = +6 V, P_{IN} = -25 dBm

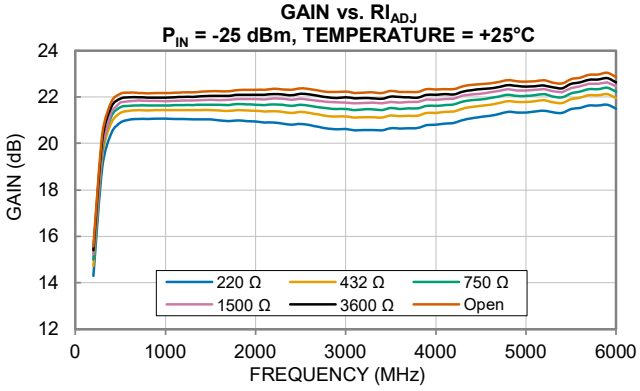


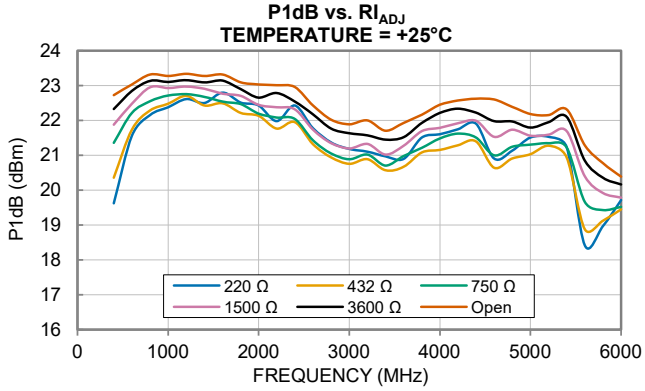
GAIN VARIATION vs. TEMPERATURE
V_{DD} = +5 V, P_{IN} = -25 dBm

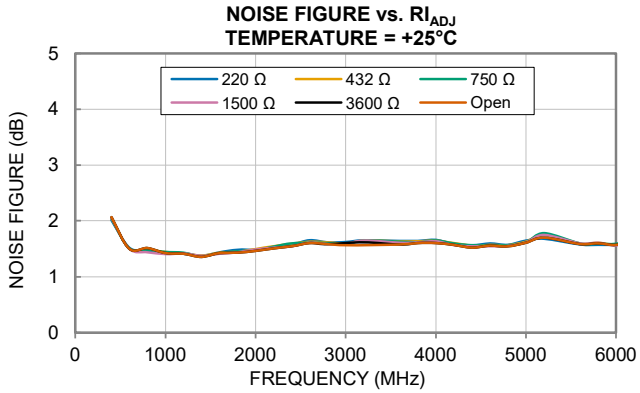


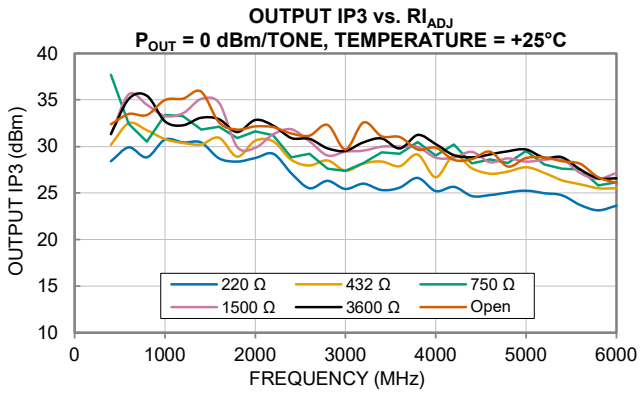
TYPICAL PERFORMANCE GRAPHS IN AMPLIFIER-ON MODE

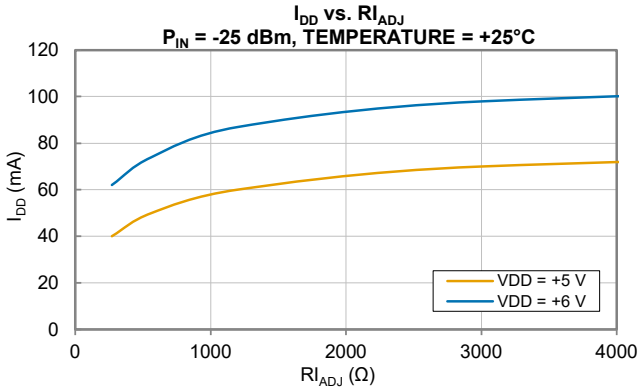
Note: The following data was taken of the packaged TSY-83LN+ mounted on Mini-Circuits Characterization Test Board TB-TSY-83LNC+ (see Figure 3). All data taken at nominal conditions V_{EN} = V_{DD} = +6 V unless noted otherwise. For additional graphs over temperature, see TSY-83LN+.





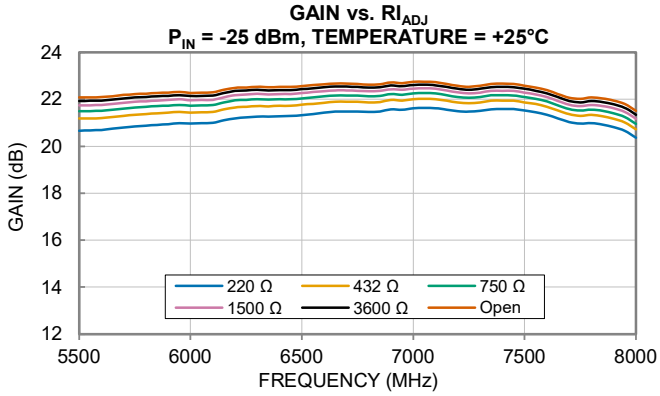


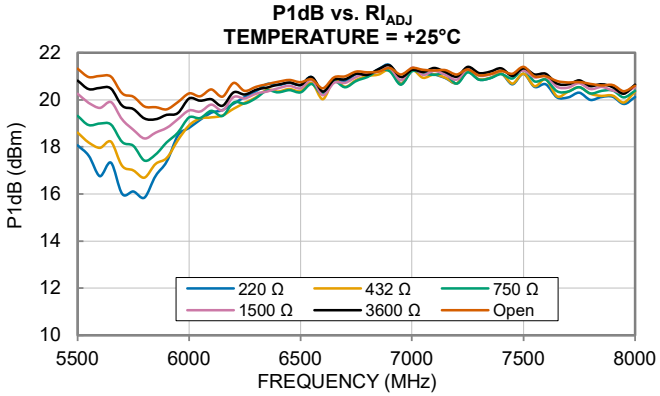


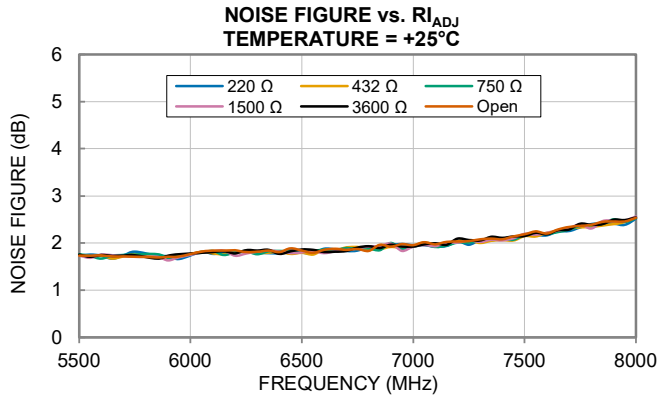


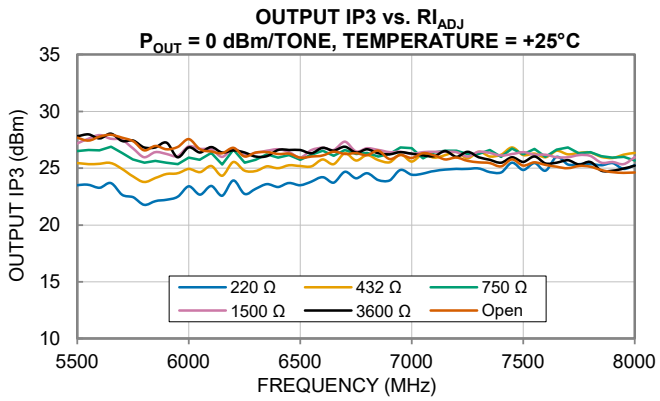
TYPICAL PERFORMANCE GRAPHS IN AMPLIFIER-ON MODE

Note: The following data was taken of the packaged TSY-83LN+ mounted on Mini-Circuits Characterization Test Board TB-TSY-832LNC+ (Figure 4). All data taken at nominal conditions $V_{EN} = V_{DD} = +6$ V unless noted otherwise. For additional graphs over temperature, see TSY-83LN+.





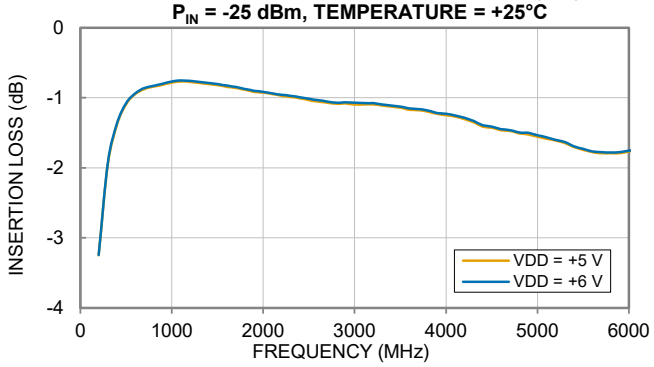




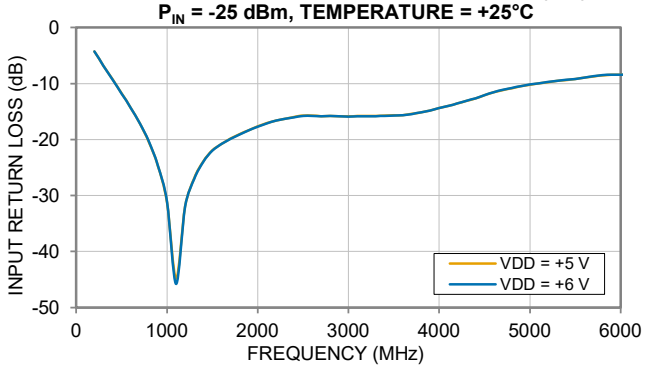
TYPICAL PERFORMANCE GRAPHS IN BYPASS MODE

Note: The following data was taken on Mini-Circuits Die Characterization 400-6000 MHz Test Board (Figure 3). All data taken at nominal conditions V_{EN} = 0 V and RI_{ADJ} = Open unless noted otherwise. For additional graphs over temperature, see TSY-83LN+.

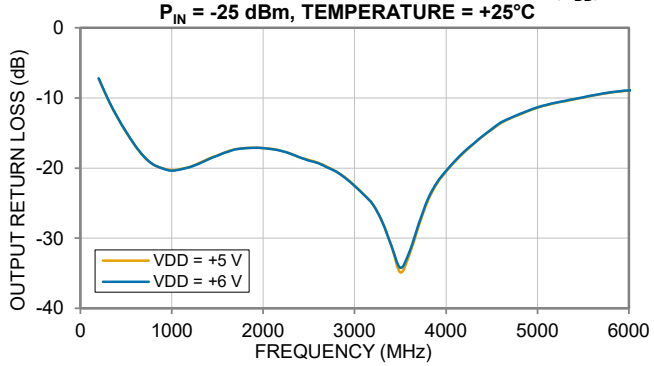
INSERTION LOSS vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



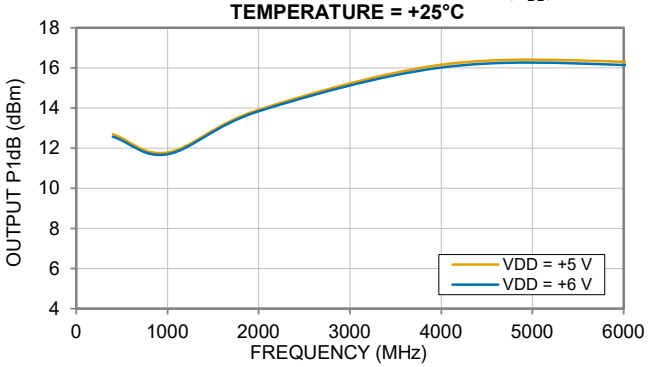
INPUT RETURN LOSS vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



OUTPUT RETURN LOSS vs. DEVICE VOLTAGE (V_{DD})
P_{IN} = -25 dBm, TEMPERATURE = +25°C



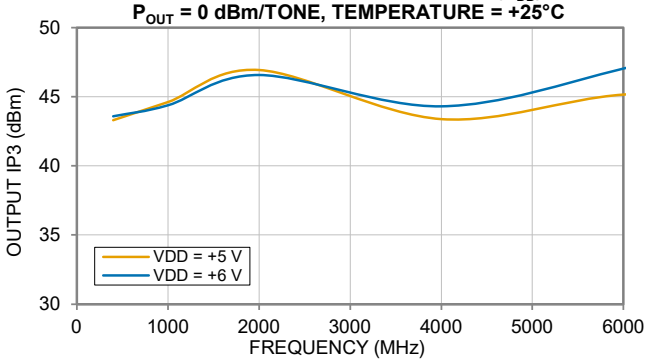
OUTPUT P1dB vs. DEVICE VOLTAGE (V_{DD})
TEMPERATURE = +25°C



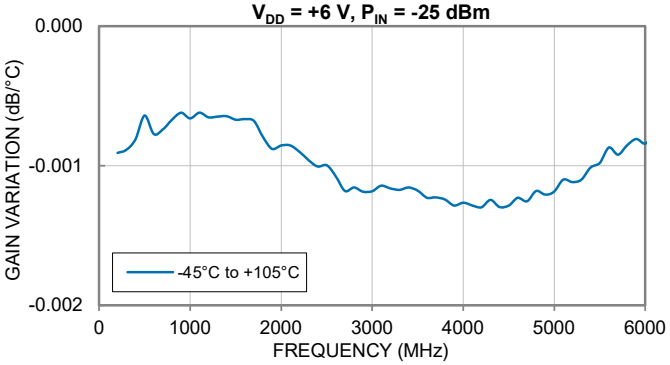
TYPICAL PERFORMANCE GRAPHS IN BYPASS MODE

Note: The following data was taken on Mini-Circuits Die Characterization 400-6000 MHz Test Board (Figure 3). All data taken at nominal conditions V_{EN} = 0 V and RI_{ADJ} = Open unless noted otherwise. For additional graphs over temperature, see TSY-83LN+.

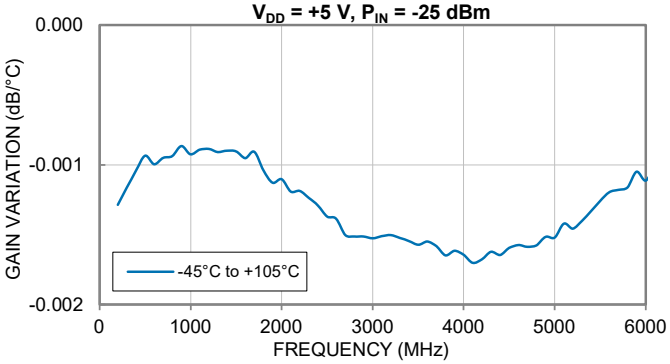
OUTPUT IP3 vs. DEVICE VOLTAGE (V_{DD})
P_{OUT} = 0 dBm/TONE, TEMPERATURE = +25°C



GAIN VARIATION vs. TEMPERATURE
V_{DD} = +6 V, P_{IN} = -25 dBm



GAIN VARIATION vs. TEMPERATURE
V_{DD} = +5 V, P_{IN} = -25 dBm



ABSOLUTE MAXIMUM RATINGS[16]

Parameter	Ratings	
Operating Temperature[17]	-45°C to +105°C	
Storage Temperature[18]	-65°C to +150°C	
Total Power Dissipation	0.83W	
Junction Temperature[19]	+150°C	
Input Power (CW)	Amplifier - ON	+22 dBm
	Amplifier - Bypass	+29 dBm
DC Voltage on RF-OUT	+14.5 V	
DC Voltage on RF-IN	+22 V	
DC Voltage on V_{DD}	+9 V	
Current I_{DD}	180 mA	
DC Voltage on V_{EN}	+9 V	
Current I_{EN}	60 mA	
Current I_{ADJ}	10 mA	

16. Permanent damage may occur if these limits are exceeded. Maximum ratings are not intended for continuous normal operation.
17. Bottom of Die.
18. For die shipped in Gel-Pak see ENV80 (limited by packaging).
19. Peak temperature at top of Die.

THERMAL RESISTANCE

Parameter	Ratings
Thermal Resistance (Θ_{JC})[20]	54.3°C/W

20. Θ_{JC}= (Hot Spot Temperature on Die - Temperature at Ground Lead)/Dissipated Power

ESD RATING[21]

	Class	Voltage Range	Reference Standard
HBM	1A	250 V to < 500 V	ANSI/ESDA/JEDEC JS-001-2017
CDM	C3	≥ 1000 V	JESD22-C101F

ESD HANDLING PRECAUTION: This device is designed to be Class 1A for HBM. Static charges may easily produce potentials higher than this with improper handling and can discharge into DUT and damage it. As a preventive measure Industry standard ESD handling precautions should be used at all times to protect the device from ESD damage.
21. ESD measured in 3x3 mm 12-Lead QFN-style package.

Low Noise Amplifier TSY-83LN-D+

50Ω 400 to 8000 MHz Bypass Mode Feature

FUNCTIONAL DIAGRAM

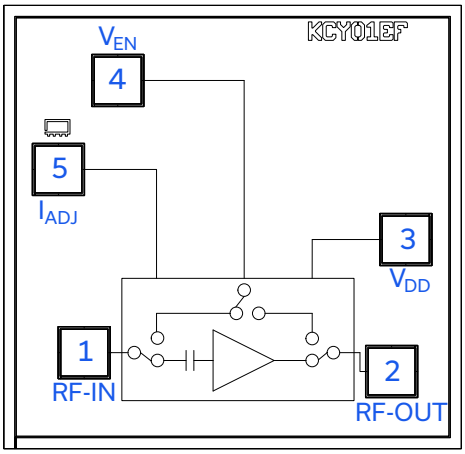


Figure 1. TSY-83LN-D+ Functional Diagram

PAD DESCRIPTION

Function	Pad Number	Description
RF-IN	1	RF-IN Pad connects to RF-Input port.
RF-OUT	2	RF-OUT Pad connects to RF-Output port.
V_{DD}	3	DC Input Pad connects to voltage input port, V_{DD}.
V_{EN}	4	DC Input Pad connects to voltage input port, V_{EN}.
I_{ADJ}[22]	5	Current Adjustment Pad connects to port, I_{ADJ}. Port left open for nominal operation. I_{ADJ} can be adjusted with the use of an external resistor (see Figures 3 and 4).
GND	Bottom of Die	Connects to ground.

22. I_{ADJ} port is not intended as a voltage input port. Permanent damage can occur if a voltage is applied to this port.

DIE OUTLINE: inches [mm], Typical

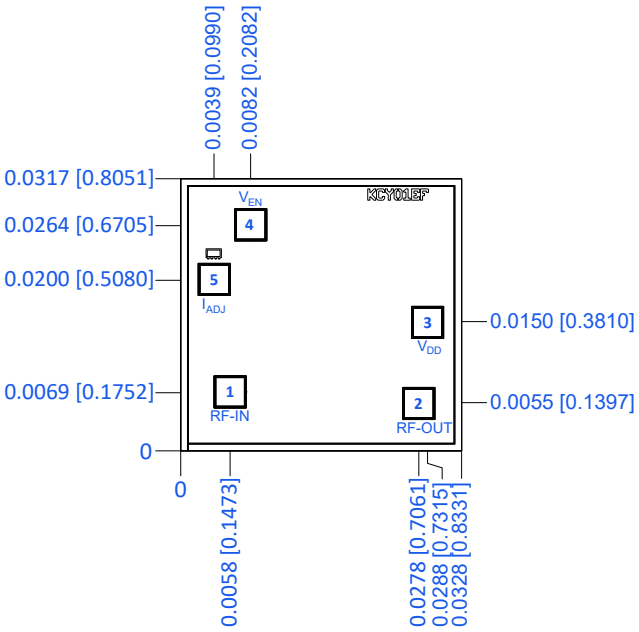


Figure 2. TSY-83LN-D+ Die Outline

DIMENSIONS: inches [mm], Typical

Die Size	0.0328 x 0.0317 [0.8331 x 0.8051]
Die Thickness	0.0040 [0.1016]
Bond Pad Size Pad 1, 2, 3, 4, 5	0.0033 x 0.0033 [0.0838 x 0.0838]
Plating (Pads & bottom of Die)	Gold

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CHARACTERIZATION BOARD

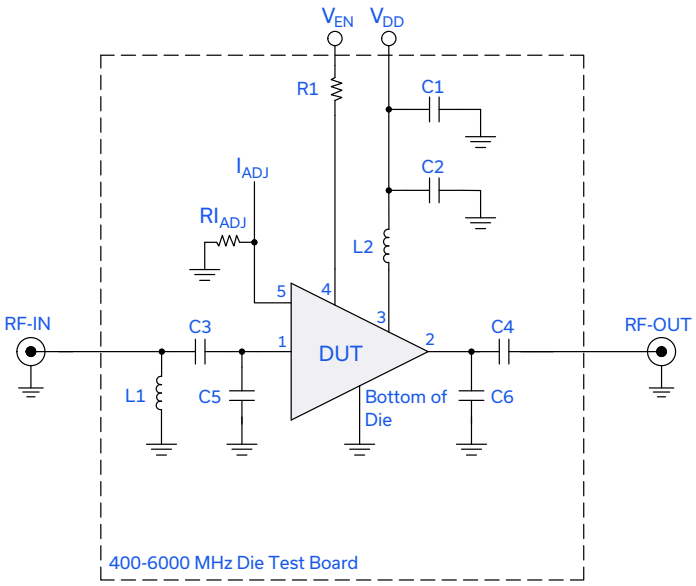

Figure 3. Wideband Die Characterization and Application Circuit. Used for characterization of device from 400 to 6000 MHz.

Electrical Parameters and Conditions
Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3),and Noise Figure measured using N5242A PNA-X Microwave Network Analyzer.

Conditions:
1. Gain and Return Loss: P_{IN} = -25 dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 0 dBm/tone at output.

Power ON/Power OFF Sequence
Caution: Permanent damage to the device will occur if the Power ON and Power OFF Sequences are not followed.

Power ON:
1) Set V_{DD} = +5 or +6 V.
2) Set V_{EN} = +5 or +6 V for Amplifier- ON Mode or V_{EN} = 0 V for Bypass Mode.
3) Turn on V_{DD} and V_{EN} (Can be turned on in any order).
4) Apply RF signal.

Power OFF:
1) Turn off RF signal.
2) Turn off V_{DD} and V_{EN} (Can be turned off in any order).

Component	Value	Size	Part Number	Manufacturer
C1	0.01 µF	0402	GRM155R71E103KA01D	Murata
C2	10 pF	0402	GJM1555C1H100JB01D	Murata
C3, C4	100 pF	0402	GRM1555C1H101JA01D	Murata
C5	0.4 pF	0402	GJM1555C1HR40WB01D	Murata
C6	0.3 pF	0402	GJM1555C1HR30WB01D	Murata
R1	0Ω	0402	RK73Z1ETTP	KOA Speer
RI_{ADJ}[23]	Not Populated	0402	--	--
L1	22 nH	0402	LQG15HS22NG02D	Murata
L2	39 nH	0402	0402CS-39NXGRW	Coilcraft

23. RI_{ADJ} resistor not needed for nominal operation. See I_{DD} versus RI_{ADJ} plot in Typical Performance Graphs section for typical current consumption.

Low Noise Amplifier TSY-83LN-D+

50Ω 400 to 8000 MHz Bypass Mode Feature

CHARACTERIZATION BOARD

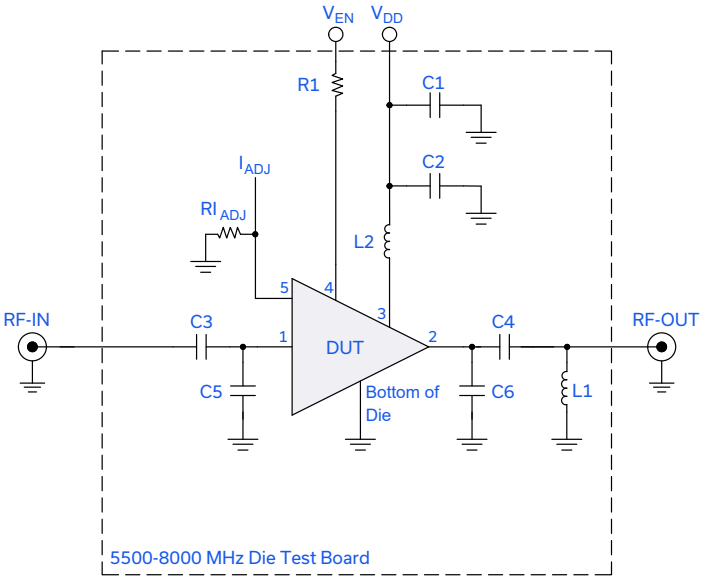

Figure 4. Narrowband Die Characterization and Application Circuit. Used for characterization of device from 5500 to 8000 MHz.

Electrical Parameters and Conditions
Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3),and Noise Figure measured using N5242A PNA-X Microwave Network Analyzer.

Conditions:
1. Gain and Return Loss: P_{IN} = -25 dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, 0 dBm/tone at output.

Power ON/Power OFF Sequence
Caution: Permanent damage to the device will occur if the Power ON and Power OFF Sequences are not followed.

Power ON:
1) Set V_{DD} = +5 or +6 V.
2) Set V_{EN} = +5 or +6 V for Amplifier- ON Mode or V_{EN} = 0 V for Bypass Mode.
3) Turn on V_{DD} and V_{EN} (Can be turned on in any order).
4) Apply RF signal.

Power OFF:
1) Turn off RF signal.
2) Turn off V_{DD} and V_{EN} (Can be turned off in any order).

Component	Value	Size	Part Number	Manufacturer
C1	0.01 µF	0402	GRM155R71E103KA01D	Murata
C2	10 pF	0402	GJM1555C1H100JB01D	Murata
C3, C4	100 pF	0402	GRM1555C1H101JA01D	Murata
C5	0.4 pF	0402	GJM1555C1HR40WB01D	Murata
C6	0.3 pF	0402	GJM1555C1HR30WB01D	Murata
R1	0Ω	0402	RK73Z1ETTP	KOA Speer
RI_{ADJ}[24]	Not Populated	0402	--	--
L1	2 nH	0402	0402CS-2N0XGRW	Coilcraft
L2	5.6 nH	0402	0402CS-5N6XGRW	Coilcraft

24. RI_{ADJ} resistor not needed for nominal operation. See I_{DD} versus RI_{ADJ} plot in Typical Performance Graphs section for typical current consumption.

ASSEMBLY DIAGRAM

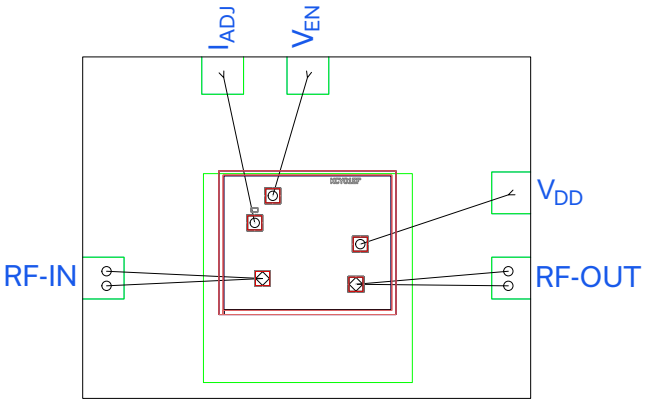

Figure 5. TSY-83LN-D+ Assembly Diagram

- Bond wire diameter: 1 mil
- Bond wire lengths from Die Pad to PCB at RF-IN port: 37 ± 2 mils
- Bond wire lengths from Die Pad to PCB at RF-OUT port: 36 ± 2 mils
- Bond wire length from Die Pad to PCB at V_{DD} port: 37 ± 2 mils
- Bond wire length from Die Pad to PCB at V_{EN} port: 29 ± 2 mils
- Bond wire length from Die Pad to PCB at I_{ADJ} port: 35 ± 2 mils
- Typical Gap from Die edge to PCB edge: 3 mils
- PCB thickness and material: 10 mils Roger RO4350B (Plating: 1 oz copper on each side)

ASSEMBLY AND HANDLING PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccator or equivalent.
2. ESD Precautions
   MMIC pHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in anti-static protected material, which should be opened only in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices require careful handling using tools appropriate for manipulating semiconductor chips. It is recommended to handle the chips along the edges with a custom designed collet. The die mounting surface must be clean and flat. Using conductive silver-filled epoxy, apply sufficient adhesive to meet the required bond line thickness, fillet height and coverage around the total periphery of the device. The recommended epoxy is Atrox 800HT5 or equivalent. Parts should be cured in a nitrogen-filled atmosphere per manufacturer's recommended cure profile.
4. Wire Bonding
   Openings in the surface passivation above the gold bond pads are provided to allow wire bonding to the die. Thermosonic bonding is recommended with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. The suggested interconnect is pure gold, 1 mil diameter wire . Bonds are recommended to be made from the bond pads on the die to the package or substrate. All bond wire length and bond wire height should be kept as short as possible, unless specified by design, to minimize performance degradation due to undesirable series inductance.

MMIC DIE

Low Noise Amplifier TSY-83LN-D+

50Ω 400 to 8000 MHz Bypass Mode Feature

ADDITIONAL DETAILED INFORMATION IS AVAILABLE ON OUR DASHBOARD CLICK HERE

Performance Data & Graphs	Data Graphs S-Parameter (S2P Files) Data Set (.zip file)	
Case Style	Die	
RoHS Status	Compliant	
Die Ordering and Packaging Information	Quantity, Package	Model No.
	Gel - Pak: 5, 10, 50, 100 KGD*	TSY-83LN-DG+
	Medium†, Partial wafer: KGD*<1892	TSY-83LN-DP+
	Full wafer†	TSY-83LN-DF+
	†Available upon request; contact sales representative. Refer to AN-60-067	
Die Marking	KCY01EF	
Environmental Ratings	ENV80	

* Known Good Die ("KGD") means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within a predefined range. While DC testing is not definitive, it does provide a high degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuits' applicable established test performance criteria and measurement instructions.

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