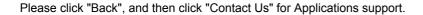
Engineering Development Model

Frequency Synthesizer

Important Note

This model has been designed, built and tested in our engineering department. Performance data represents model capability. At present it is a non-catalog model. On request, we can supply a final specification sheet, part number and price/delivery information.



ZSN-EDR11277



CASE STYLE: KH1331

ELECTRICAL SPECIFICATIONS 50Ω, over -15°C to +75°C							
Parameter	Min.	Тур.	Max.	Units			
Frequency	1380		1480	MHz			
Step size		100		kHz			
Settling Time Within ±1kHz		9		msec			
Output Power	+7	+11	+15	dBm			
Phase Noise							
at 10	0 Hz offset	-89		dBc/Hz			
at 1	kHz offset	-90		dBc/Hz			
at 10	KHz offset	-97		dBc/Hz			
at 100	KHz offset	-90	-119	dBc/Hz			
at 1000	kHz offset	-145	-139	dBc/Hz			
Integrated SSB Phase Noise		-49		dBc			
Ref & Comp Spurious Suppression	1	-82		dBc			
0.5 Step size Spurious Suppression	n	-91		dBc			
Non-Harm. Spurious Suppression		-90		dBc			
Harmonic Suppression		-31		dBc			
Supply voltage VCO &	PLL	12		V			
Supply current VCO &	PLL	13	21	V			
Freque	ncy	10		MHz			
Reference In Amplit	ude	1		Vp-p			
(External) Impeda	ince	100		kΩ			
Ph. N @	1kHz	-145		dBc/Hz			
Input Logic Logic I	nigh 1.4		3.33	V			
Levels Logic I	_ow		0.6	V			
Digital Lock Lock	ed 1.4		3.33	V			
Detect Unlock	ked		0.4	V			
Frequency Synthesizer PLL		ADF4153					

ABSOLUTE MAXIMUM RATINGS					
Operating Temperature	-45°C to 85°C				
Storage Temperature	-55°C to 100°C				
Supply Voltage	13V				
Reference Frequency voltage	3.6Vp-p				
Data, Clock & LE levels	3.63V				

D-Sub15(Male) Pin connections			Other Connections		
VCC PLL	6	CLOCK	2	RF OUT	SMA (Female)
VCC VCO	8	DATA	3	REF IN	SMA (Female)
LOCK DETECT	1	LATCH ENABLE	4		
NOT CONNECTED	9-15	GROUND	5,7		