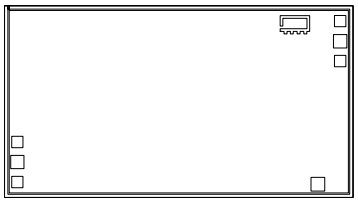
MMIC DIE

Wideband Amplifier AVA-5R183-D+

50Ω 0.5 to 18 GHz

THE BIG DEAL

- Wideband, 0.5 to 18 GHz
- Excellent Gain Flatness, ±1.6 dB Typ. up to 18 GHz
- Good Reverse Isolation, 36 dB Typ.
- +18 dBm Typ. P1dB.



+RoHS Compliant
The +Suffix identifies RoHS Compliance.
See our website for methodologies and qualifications

SEE ORDERING INFORMATION ON THE LAST PAGE

APPLICATIONS

- 5G MIMO and Back Haul Radio Systems
- Satellite Ka-band Communications
- Test and Measurement Equipment
- Radar, EW, and ECM Defense Systems

PRODUCT OVERVIEW

The AVA-5R183-D+ is a GaAs PHEMT MMIC wideband amplifier operating from 0.5 to 18 GHz. The amplifier provides 13.5 dB of Gain, +18 dBm P1dB, and +23 dBm OIP3 typical performance while operating from a +5V supply with 85 mA current consumption. The amplifier has excellent input and output impedance matches which makes for easy cascading with other devices in multi-chip modules. The Gain flatness along with the other performance characteristics makes AVA-5R183-D+ ideal for use in wideband EW Defense Systems and Test and Measurement Equipment.

KEY FEATURES

Features	Advantages
Wideband: 0.5 to 18 GHz	General purpose wideband amplifier is suitable for wide variety of applications.
Excellent Gain Flatness • 1.6 dB Typ. up to 18 GHz	Desirable feature for maintaining frequency response within wideband signal chains.
Good Reverse Isolation, 18 dB Typ.	Isolates adjacent circuitry without need for an external expensive isolator.
Good Input and Output Return Loss	Excellent Return Loss enables easy cascade within wideband signal chains.
Unpackaged die	Suitable for chip and wire hybrid assemblies.

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ELECTRICAL SPECIFICATIONS[1] AT 25°C, VDD = +5V, IDD = 85mA & Zo = 50Ω, UNLESS NOTED OTHERWISE

Parameter	Condition (GHz)	VDD = +5V			Units
		Min.	Typ.	Max.	
Frequency Range		0.5		18	GHz
Gain	0.5		14.6		dB
	5		12.9		
	10		13.3		
	15		12.5		
	18		13.1		
Input Return Loss	0.5		12		dB
	5		12		
	10		13		
	15		9		
	18		12		
Output Return Loss	0.5		36		dB
	5		25		
	10		34		
	15		16		
	18		17		
Reverse Isolation	0.5-18		36		dB
Output Power at 1 dB Compression	0.5		19.5		dBm
	5		19.7		
	10		18.6		
	15		17.7		
	18		16.3		
Output Third-Order Intercept Pout = 0 dBm/Tone	0.5		31.3		dBm
	5		27.4		
	10		23.3		
	15		21.7		
	18		20		
Noise Figure	0.5		4.8		dB
	5		3.3		
	10		2.8		
	15		3.6		
	18		4.4		
Device Operating Voltage (VDD)		+4.75	+5	+5.25	V
Device Operating Current (IDD)			85		mA
Device Gate Voltage (VG)			-0.94		V
Device Gate Current (IG)			0.47		µA
Device Current Variation vs. Temperature[2]			264.5		µA/°C
Device Current Variation vs. Voltage[3]			0.007		mA/mV
Thermal Resistance, Junction-to-Ground Lead (ΘJC)			22.2		°C/W

1. Die is soldered and measured on a die characterization board. See characterization circuit (Fig. 1)
2. Device Current Variation vs. Temperature = (Current in mA at +100°C – Current in mA at -55°C) / +155°C
3. Device Current Variation vs. Voltage = (Current in mA at +5.25V – Current in mA at +4.75V) / ((+5.25V – +4.75V) * 1000 mA/mV)

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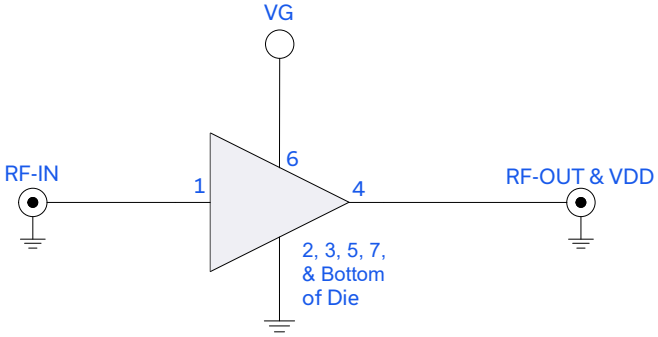
MAXIMUM RATINGS[4]

Parameter	Ratings
Operating Temperature (ground lead)	-55°C to +100°C
Junction Temperature	+150°C[5]
Power Dissipation	4.4W[6]
Input Power (CW)	+22 dBm
DC Voltage on RF-OUT & VDD	+7V
DC Voltage on VG	-0.5V to -2V
DC Voltage on RF-IN[7]	+7V
Current IDD	250mA
Current IG	2mA

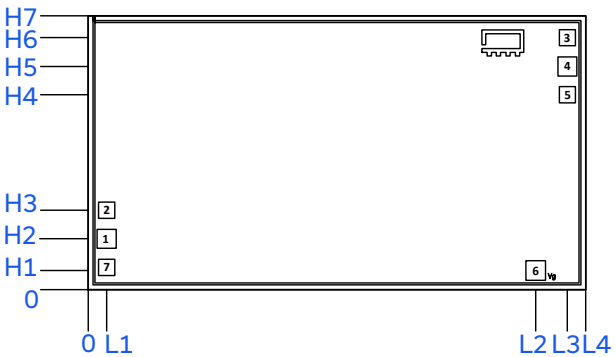
4. Permanent damage may occur if these limits are exceeding. Electrical maximum ratings are not intended for continuous normal operation
5. Tj = +85°C + (VDD)*(IDD)*(ΘJC) = +94°C. Keeping Tj below +94°C will ensure MTTF > 100 Years.
6. Derates linearly to 1.57 W at +100°C
7. DC signal at RF-IN will be blocked by internal blocking capacitor. However, a DC current of 3.5µA will be present due to the input shunt resistor assuming VRF-IN = +7V.

SIMPLIFIED SCHEMATIC AND PAD DESCRIPTION



Function	Pad Number	Description
RF-IN	1	RF Input Pad
RF-OUT & VDD	4	RF Output and DC Input Pad
VG	6	Gate Bias Pad
GROUND	2,3,5,7 & Bottom of Die	The bond pads are connected to back-side through vias and do not require any wire-bond connections to ground.

BONDING PAD POSITION



DIMENSIONS IN µm, TYP.

L1	L2	L3	L4
96	2351	2518	2614

H1	H2	H3	H4	H5	H6	H7
99	267	417	1024	1172	1324	1438

Thickness	Die size	Pad size 1,4 & 6	Pad size 2,3,5,7
100	2614 x 1438	100 x 100	85 x 85

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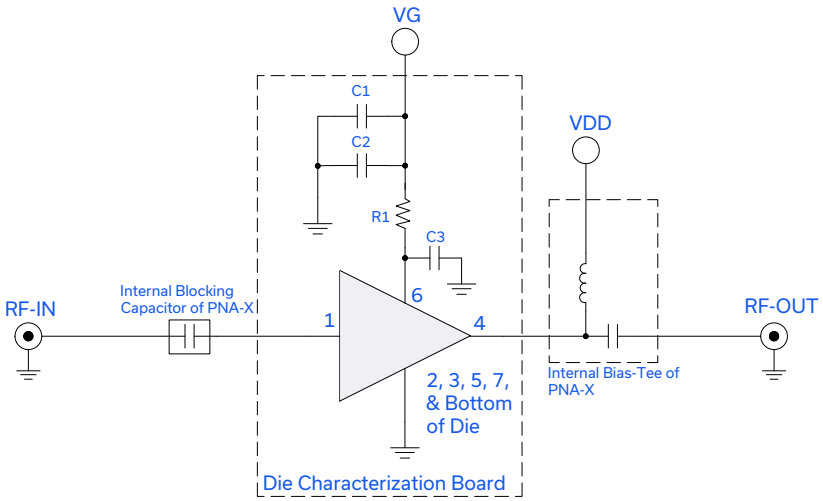
CHARACTERIZATION & APPLICATION CIRCUIT



Component	Size	Value	Part Number	Manufacturer
R1	0402	1K Ohm	FC0402E1001DTT5	Vishary
C1	0402	100pF	GRM1555C1H101JA01J	Murata
C2	0402	0.1uF	GRM155R71C104KA88D	Murata
C3	Chip Capacitor	100pF	MA4M3100	MACOM

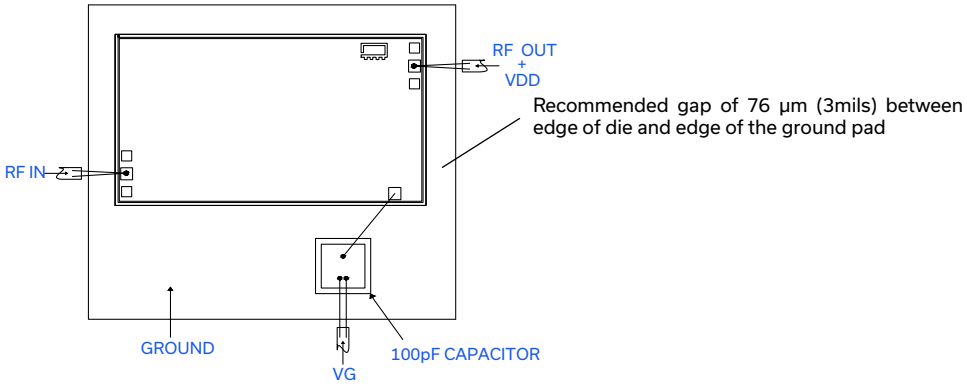
Fig 1. Characterization & Application Circuit
Note: This block diagram is used for characterization, (Die is attached and wire-bonded on die characterization test board). Gain, Return Loss, Output Power at 1dB Compression (P1dB), Output IP3 (OIP3) and Noise Figure are measured using Agilent's N5242A PNA- X Microwave Network Analyzer.

Conditions:
1. VDD = +5V
2. VG is set to obtain desired IDD as shown in specification table.
3. Gain and Return Loss: Pin= -25 dBm
4. Output IP3 (OIP3): Two Tones, spaced 1 MHz apart, 0 dBm/Tone at output.

Switch ON/OFF sequence:
1. To switch the amplifier ON:
   a. Set VG = -1.1V. Apply VG.
   b. Set VDD = +5V. Apply VDD.
   c. Increase VG to obtain desired IDD as shown in specification table.
   d. Apply RF signal

2. To switch the amplifier OFF:
   a. Turn OFF RF signal
   b. Adjust VG down to -1.1V.
   C. Turn off VDD.
   D. Turn off VG.

ASSEMBLY DRAWING



Note: Tested on die characterization board with following bond lengths:
1. Bond length for RF-IN: 330 µm (13 mils)
2. Bond length for RF-OUT + VDD: 330 µm (13 mils)
3. Bond lengths from die, capacitor, and VG were kept as short as possible

ASSEMBLY PROCEDURE

1. Storage
   Die should be stored in a dry nitrogen purged desiccators or equivalent.
2. ESD
   MMIC PHEMT amplifier die are susceptible to electrostatic and mechanical damage. Die are supplied in antistatic protected material, which should be open in clean room conditions at an appropriately grounded anti-static workstation.
3. Die Handling and Attachment
   Devices need careful handling using correctly designed collets, it is recommended to handle the chip along the edges with a custom design collet. The die mounting surface must be clean and flat. Using conductive silver filled epoxy, recommended epoxies are Ablestik 84-1 LMISR4 or equivalents. Apply sufficient epoxy to meet required epoxy bond line thickness, epoxy fillet height and epoxy coverage around total periphery. Parts shall be cured in a nitrogen filled atmosphere per manufacturer's cure condition. The surface of the chip has exposed air bridges and should not be touched with vacuum collet, tweezers or fingers.
4. Wire Bonding
   Bond pad openings in the surface passivation above the bond pads are provided to allow wire bonding to the die gold bond pads. Thermo-sonic bonding is used with minimized ultrasonic content. Bond force, time, ultrasonic power and temperature are all critical parameters. Suggested wire is pure gold, 1mil diameter. Bonds must be made from the bond pads on the die to the packaged or substrate. All bond wire length and bond wire height should be kept as short as possible unless specified by the Assembly Drawing to minimize performance degradation due to undesirable series inductance.

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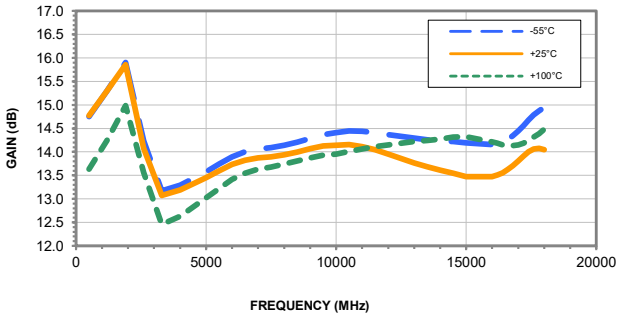
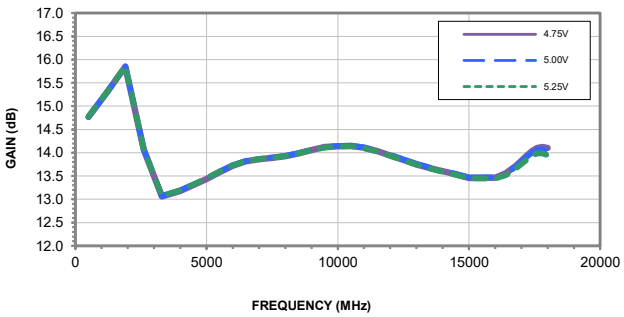
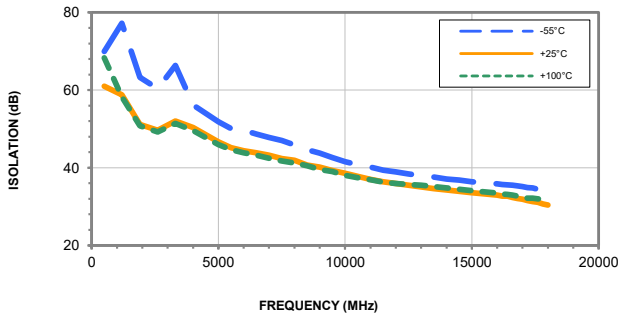
GAIN vs. FREQUENCY & TEMPERATURE
INPUT POWER = -25 dBm, VDD = +5V



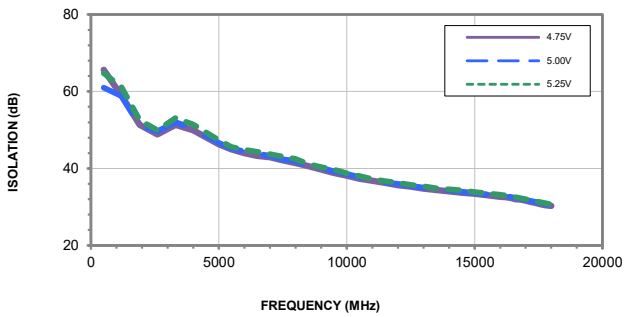
GAIN vs. FREQUENCY & DEVICE VOLTAGE
INPUT POWER = -25 dBm, Temperature = +25°C



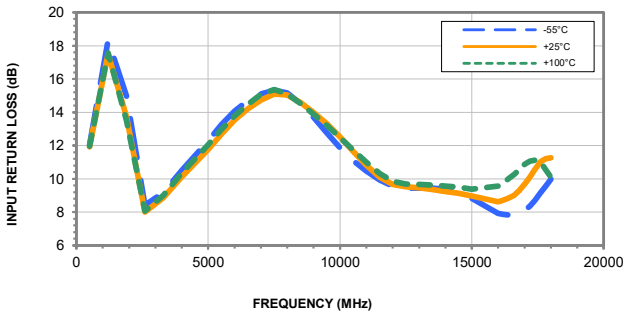
ISOLATION vs. FREQUENCY & TEMPERATURE
INPUT POWER = -25 dBm, VDD = +5V



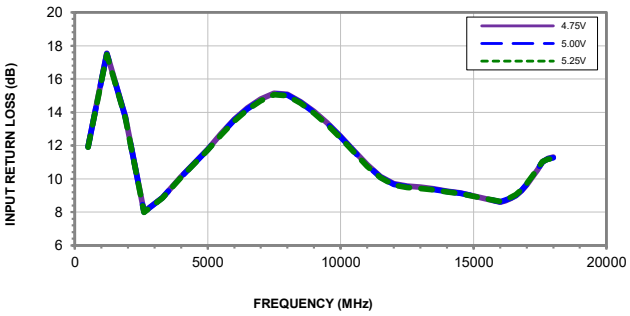
ISOLATION vs. FREQUENCY & DEVICE VOLTAGE
INPUT POWER = -25 dBm, Temperature = +25°C



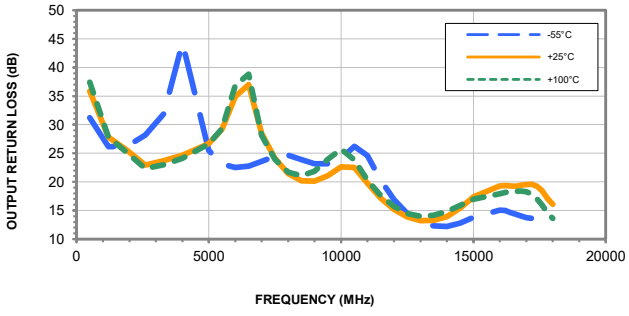
INPUT RETURN LOSS vs. FREQ. & TEMP.
INPUT POWER = -25 dBm, VDD = +5V



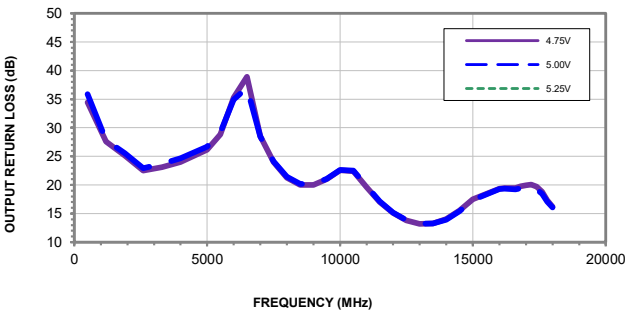
INPUT RETURN LOSS vs. FREQ. & DEVICE VOLTAGE
INPUT POWER = -25 dBm, Temperature = +25°C



OUTPUT RETURN LOSS vs. FREQ. & TEMP.
INPUT POWER = -25 dBm, VDD = +5V



OUTPUT RETURN LOSS vs. FREQ. & DEVICE VOLTAGE
INPUT POWER = -25 dBm, Temperature = +25°C



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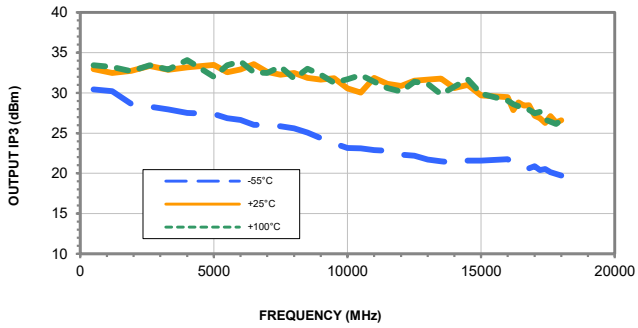
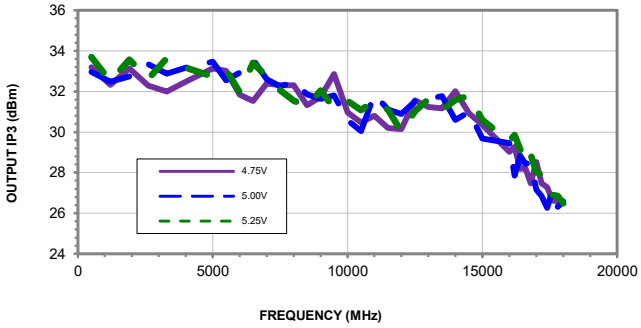
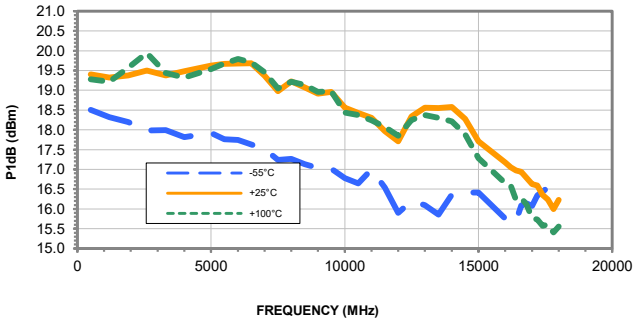
OUTPUT IP3 vs. FREQUENCY & TEMPERATURE
OUTPUT POWER = -5 dBm, VDD = +5V



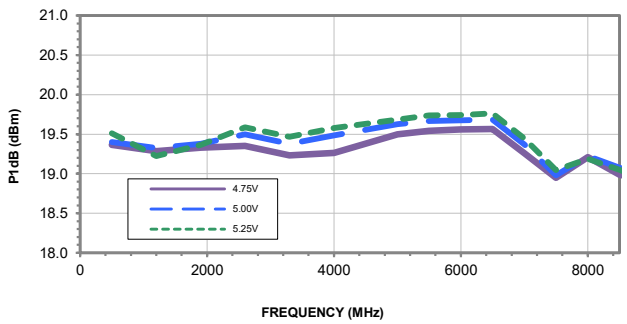
OUTPUT IP3 vs. FREQUENCY & DEVICE VOLTAGE
OUTPUT POWER = -5 dBm, Temperature = +25°C



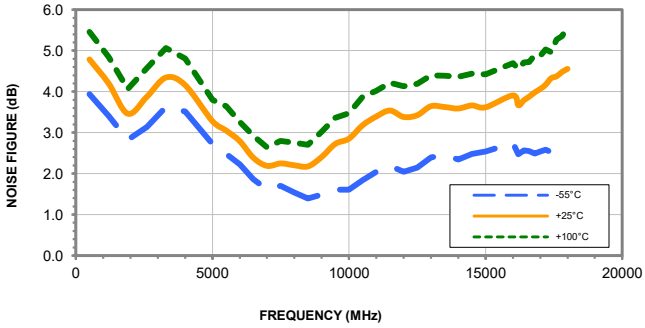
P1dB vs. FREQUENCY & TEMPERATURE
VDD = +5V



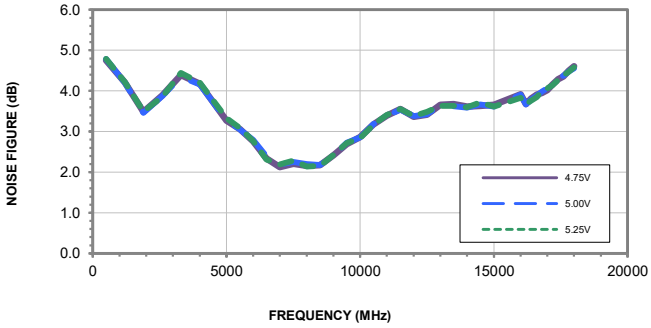
P1dB vs. FREQUENCY & DEVICE VOLTAGE
Temperature = +25°C



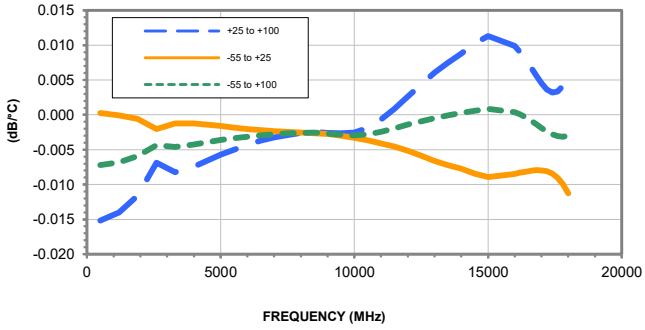
NOISE FIGURE vs. FREQUENCY & TEMPERATURE
VDD = +5V



NOISE FIGURE vs. FREQUENCY & DEVICE VOLTAGE
Temperature = +25°C



GAIN VARIATIONS VS FREQUENCY & TEMPERATURE
INPUT POWER = -25 dBm, VDD = +5V



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ADDITIONAL DETAILED TECHNICAL INFORMATION IS AVAILABLE ON OUR DASH BOARD.

Performance Data	Data Table Swept Graphs S-Parameter (S2P Files) Data Set with and without port extension(.zip file)	
Case Style	Die	
Die Ordering and packaging information	Quantity, Package Gel – Pak: 5, 10, 50, 100, 200 Medium†, Partial wafer: KGD*<2565 Full Wafer †Available upon request contact sales representative Refer to AN-60-067	Model No. AVA-5R183-DG+ AVA-5R183-DP+ AVA-5R183-DF+
Die Marking	EL-AMP-5-2	
Environmental Ratings	ENV80	

*Known Good Die ('KGD') means that the die in question have been subjected to Mini-Circuits DC test performance criteria and measurement instructions and that the parametric data of such die fall within predefined range. While DC testing is not definitive, it does provide a higher degree of confidence that die are capable of meeting typical RF electrical parameters specified by Mini-Circuits.

NOTES

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