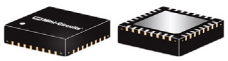
Digital Controlled Variable Gain Amplifier DVGA3-122+

50Ω 0.9 to 1.2 GHz
31.5 dB, 0.5 dB Step, 6 Bit Serial Control

The Big Deal

- Integrated Amplifier, Reflectionless Filter and Digital Attenuator
- 20 dB Gain / 31.5 dB Gain Control
- Flat frequency response, ±0.85 dB (0.9-1.2 GHz)



CASE STYLE: DG1677-2

Product Overview

The DVGA3-122+ is a multi-chip module that consists of a low noise amplifier, a voltage control attenuator with 6-bit serial control and a low pass reflection-less filter. It operates on a single 5v supply and well matched for 50Ω. It comes in a tiny, low profile package (5x5x0.89mm), accommodating dense circuit board layouts.

Key Features

Feature	Advantages
31.5 dB attenuation in 0.5 dB step size	Combining medium gain and a wide range of gain control makes the DVGA3-122+ an ideal building block for any RF chain where level setting control is required in a small space.
Flat frequency response, ±0.85 dB over 0.9-1.2 GHz	No need for external components to flatten gain.
Medium Gain, 20 dB	Incorporating multiple stages of amplification, the DVGA3-122+ provides medium gain over a wideband reducing cost and PCB board space.
Good IP3, +28 dBm at 1.0 GHz	Use in receivers and transmitters giving the users advantage in instantaneous spur free dynamic range over wide bandwidths.
Output Power, +15.6 dBm at 1.0 GHz	The DVGA3-122+ maintains consistent output power capability over the full attenuation range and operating temperature range making it ideal to be used in remote applications such as LNB's as the L Band driver stage.
5x5 mm 32-lead MCLP package	Tiny footprint saves space in dense layouts while providing low inductance, repeatable transitions, and excellent thermal contact to the PCB.

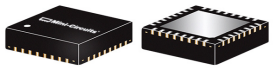
Digital Controlled Variable Gain Amplifier

50Ω 0.9 - 1.2 GHz

20 dB Gain, 0.5 dB Step, 31.5 dB Attenuation, 6 Bit Serial Control

Product Features

- 31.5 dB Gain control 0.5dB step size
- Gain, 20 dB typ. at 1 GHz
- Serial control interface
- Small size 5.0 x 5.0 mm



Generic photo used for illustration purposes only

DVGA3-122+

CASE STYLE: DG1677-2

+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

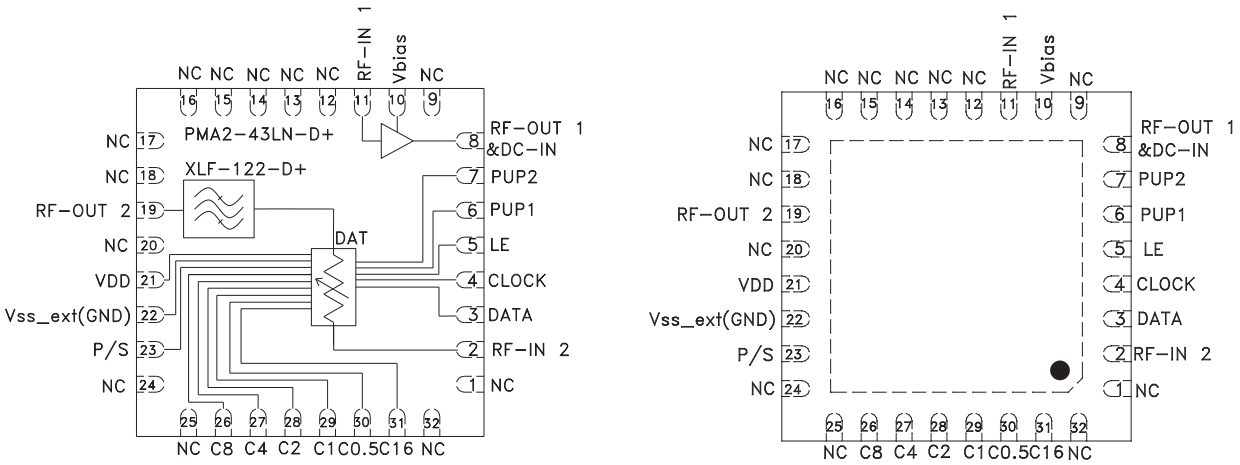
Typical Applications

- Radio Location
- Fixed Satellite
- Space Research

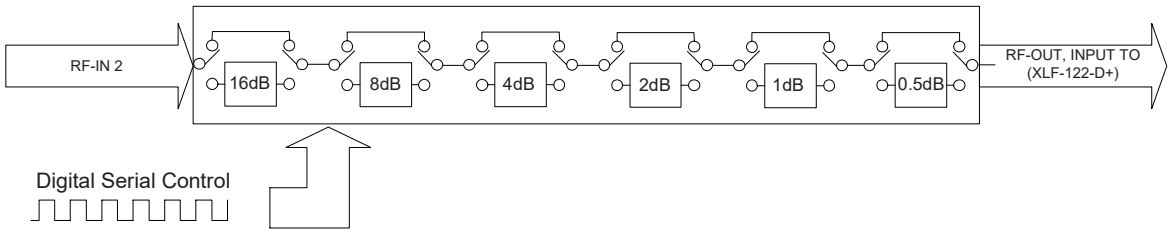
General Description

The DVGA3-122+ is a multi-chip module that consists of a low noise amplifier, a voltage control attenuator with 6-bit serial control and a low pass reflection-less filter. It operates on a single 5v supply and well matched for 50Ω. It comes in a tiny, low profile package (5x5x0.89mm), accommodating dense circuit board layouts.

Simplified Schematic of DUT



Simplified Schematic of DAT



Pad Description (Table 1)

Pad Number	Function	Pad Description (See Figure 1 for TB-DVGA3-122+ Drawing)
2	RF-IN 2	RF Input Pad of the Digital Control Attenuator (DAT) (Note 1)
3	DATA	Data Pad of DAT (Note 3)
4	CLOCK	Clock Pad of DAT
5	LE	Latch Enable Pad of DAT (Note 2)
6	PUP1	Power Up Pad of DAT. Grounded externally on Test Board via 10K Resistor(R15)
7	PUP2	Power Up Pad of DAT. Grounded externally on Test Board via 10K Resistor(R14)
8	RF-OUT 1 &DC-IN	RF Output & DC Supply Pad of Amplifier. Connects to VS per Figure 1.
10	Vbias	Biasing Voltage Pad of Amplifier. Connects to VS per Figure 1.
11	RF-IN 1	RF Input Pad of Amplifier. Connects to Vbias per Figure 1.
19	RF-OUT 2	RF Output Pad of Reflection-less Low Pass Filter (Note 1)
21	VDD	DC Supply Pad of DAT. Connects to VS per Figure 1
22	Vss_ext(GND)	Control pad to internal negative voltage generator of DAT. Connects to ground per Figure 1
23	P/S	P/S Pad of DAT. Connects to VS per Figure 1
26	C8	Attenuation Control Bit (8dB). Connects to ground via a 10Kohm Resistor (Note 4)
27	C4	Attenuation Control Bit (4dB). Connects to ground via a 10Kohm Resistor (Note 4)
28	C2	Attenuation Control Bit (2dB). Connects to ground via a 10Kohm Resistor (Note 4)
29	C1	Attenuation Control Bit (1dB). Connects to ground via a 10Kohm Resistor (Note 4)
30	C0.5	Attenuation Control Bit (0.5dB). Connects to ground via a 10Kohm Resistor (Note 4)
31	C16	Attenuation Control Bit (16dB). Connects to ground via a 10Kohm Resistor (Note 4)
1,9,12-18,20,24, 25 &32	NC	Not Connected. Grounded on test board.
Paddle	Ground	Ground (Note 5).

Notes:
1. RF input and output ports shall be AC coupled with external blocking capacitor.
2. Latch Enable (LE) has an internal 2MΩ pull-up resistor to VDD (Pin 21).
3. Place a shunt 10KΩ resistor to avoid freq. resonance (see layout drawing PL-655).
4. Refer to Power-up Control Settings.
5. The exposed solder pad on the bottom of the package (See Pin Configuration) must be grounded for proper device operation.
6. See application and characterization test circuit Fig. 1 and layout drawing PL-655.

RF Electrical Specifications[1] at 25°C, 50Ω With Vs=5V

Parameter	Condition (MHz)	Min.	Typ.	Max.	Units
Frequency Range		900		1200	MHz
Gain (at 0 dB attenuation)	900	18.3	20.4	22.4	dB
	1000	18.0	20.0	22.0	
	1100	17.5	19.4	21.3	
	1200	16.8	18.7	20.6	
Input Return Loss (all states)	900		7		dB
	1000		9		
	1100		10		
	1200		11		
Output Return Loss (all states)	900		6		dB
	1000		7		
	1100		8		
	1200		9		
Output Power @ 1 dB compression (at 0 dB attenuation)	900		15.4		dBm
	1000		15.6		
	1100		15.7		
	1200		15.7		
Output IP3 (at 0 dB attenuation)	900		27.0		dBm
	1000		28.0		
	1100		28.2		
	1200		28.1		
Noise Figure (at 0 dB attenuation)	900		0.5		dB
	1000		0.5		
	1100		0.5		
	1200		0.5		
Accuracy @ 0.5 dB Attenuation Setting	900 - 1200		0.07	0.4	dB
Accuracy @ 1 dB Attenuation Setting	900 - 1200		0.11	0.5	dB
Accuracy @ 2 dB Attenuation Setting	900 - 1200		0.03	0.3	dB
Accuracy @ 4 dB Attenuation Setting	900 - 1200		0.05	0.3	dB
Accuracy @ 8 dB Attenuation Setting	900 - 1200		0.01	0.5	dB
Accuracy @ 16 dB Attenuation Setting	900 - 1200		0.11	0.8	dB
Supply Voltage (Vs)	DC	4.75	5.0	5.25	V
Supply Current (Is)	DC		52.2	64.2	mA
Current Variation vs. Temperature[2]			-29.5		mA/° C
Current Variation vs. Voltage[3]			0.015		mA/mV
Thermal Resistance, Junction to ground lead (Amplifier)		—	61	—	°C/W

1. Measured in Mini-Circuits characterization test board TB-DVGA3-122+. See characterization Test Circuit (Fig. 1)
2. Device Current Variation vs. Temperature = (Current at 85°C – Current at -45°C)/ 130°C
3. Device Current Variation vs. Voltage = (Current at 5.25V –Current at 4.75V)/(5.25V-4.75V)

Absolute Maximum Ratings[4]

Parameter	Ratings
Operating Temperature (ground pad)	-40°C to 85°C
Storage Temperature	-65°C to 150°C
Supply Voltage Vs	5.5V Max.
Input Power	XLF-122-D+ at Passband: +33 dBm PMA2-43LN-D+: +22 dBm DAT: +30 dBm
Total Power Dissipation	PMA2-43LN-D+: 0.7W DAT: 1W

4. Permanent damage may occur if any of these limits are exceeded.

Control Voltage[5]

Parameter	Min.	Typ.	Max.	Units
Control Input Low	-0.3	—	0.6	V
Control Input High	1.17	—	3.6	V
Control Current[6]	—	—	20	mA

5. Applicable to Data (Pad#3), Clock (Pad#4), LE (Pad#5), PUP1 (Pad#6), PUP2 (Pad#7), C0.5-C16 (Pad#27-31).
6. Except 30mA typ. for C0.5, C16

Attenuation Switching Specifications

Parameter	Min.	Typ.	Max.	Units
Switching Speed, 50% Control to 0.5dB of Attenuation Value	—	1.0	—	mSec
Switching Rep Rate	—	—	25	KHz

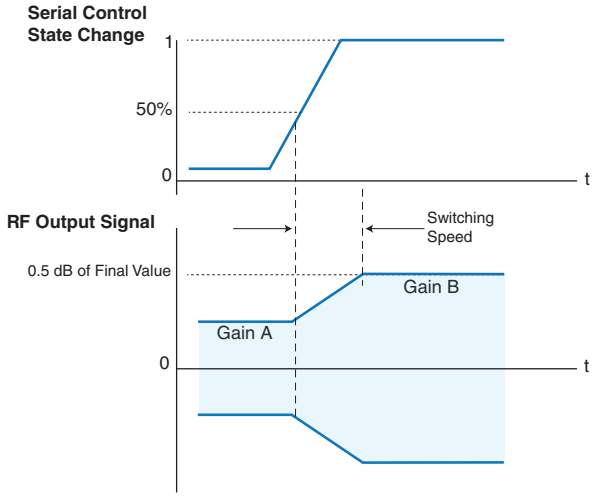
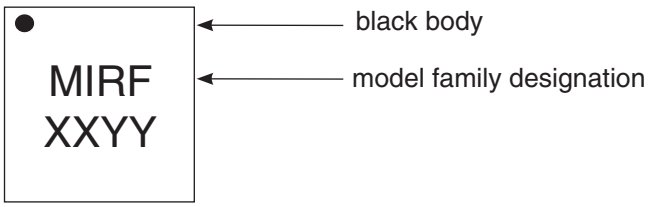


Table 2. Truth Table

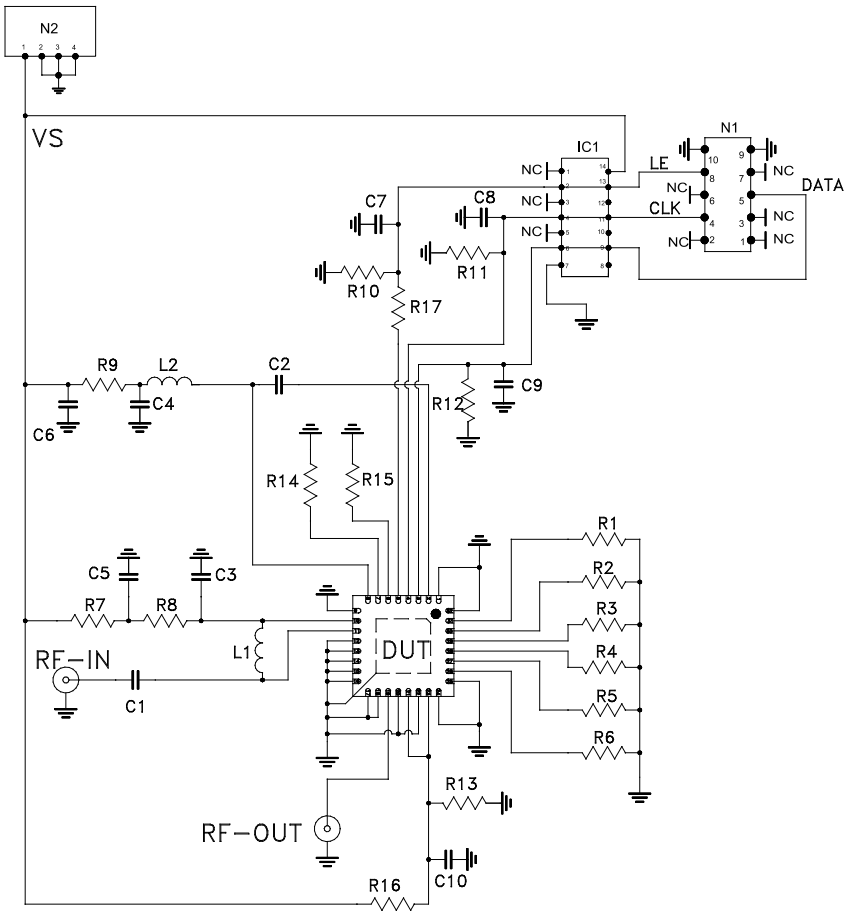
Attenuation State	C16	C8	C4	C2	C1	C0.5
Reference	0	0	0	0	0	0
0.5 (dB)	0	0	0	0	0	1
1 (dB)	0	0	0	0	1	0
2 (dB)	0	0	0	1	0	0
4 (dB)	0	0	1	0	0	0
8 (dB)	0	1	0	0	0	0
16 (dB)	1	0	0	0	0	0
31.5 (dB)	1	1	1	1	1	1
Note: Not all 64 possible combinations of C0.5 - C16 are shown in table						

The serial interface is a 6-bit serial in, parallel-out shift register buffered by a transparent latch. It is controlled by three CMOS-compatible signals: Data, Clock, and Latch Enable (LE). The Data and Clock inputs allow data to be serially entered into the shift register, a process that is independent of the state of the LE input. The LE input controls the latch. When LE is HIGH, the latch is transparent and the contents of the serial shift register control the attenuator. When LE is brought LOW, data in the shift register is latched. The shift register should be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data. The timing for this operation is defined by Figure 2 (Serial Interface Timing Diagram) and Table 3 (Serial Interface AC Characteristics).

Product Marking



Application and Characterization Test Circuit



Component	Size	Value	P/N	Manufacturer
DUT	5x5mm	Amplifier	DVGA3-122+	MCL
IC1	--	Hex Inverting Schmitt Trigger	MM74HC14M	Fairchild Semiconductor
N1	--	Vertical Breakaway Header 10 Circuits	015-91-0100	Molex
N2	--	Vertical Header 4 Circuits	53398-0471	Molex
C1,C2	0402	0.001uF	GRm1555C1H102JA01D	Murata
C3,C4	0402	100pF	04025A101JAT2A	AVX or Equivalent
C5,C6	0603	4.7uF	JMK105BBJ475MV-F	Taiyo Yuden Inc.
C7,C8,C9	0603	100pF	GRM1885C1H101JA01D	Murata
C10	0805	0.47uF	TMCP1D104KTRXF	Holy Stone
R1-R6	0603	10KOhm	RK73H1JTTD1002F	KOA
R7	0402	5.11kOhm	RK73H1ETTP5111F	KOA
R8	0805	49.9Ohm	RK73H1ETTP49R9F	KOA
R9	0603	0 Ohm	KR73Z1JTTD	KOA
R10-R12,R14&R15	0603	10KOhm	RK73H1JTTD1002F	KOA
R13	0603	681Ohm	RK73H1JTTD4750F	KOA
R16	0603	475Ohm	RK73H1ETTP6810F	KOA
L1	0402	10nH	LQW15AN10NH00D	Murata
L2	0402	8.2nH	LQW15AN8N2G00D	Murata
R17	0805	10KOhm	RK73H2ATTD1002F	KOA

Figure 1. Block diagram of Test Circuit used for characterization. (DUT soldered on Mini-Circuits Characterization Test Board TB-DVGA3-122+). Gain, Return Loss, Output power at 1dB Compression (P1dB), Output IP3 and noise figure are measured using Agilent's N52244A-PNA-X Microwave network analyzer.
Condition:
1. Gain and Return Loss: Pin=-25 dBm
2. Output IP3 (OIP3): Two tones, spaced 1 MHz apart, +5dBm/Tone at Output.

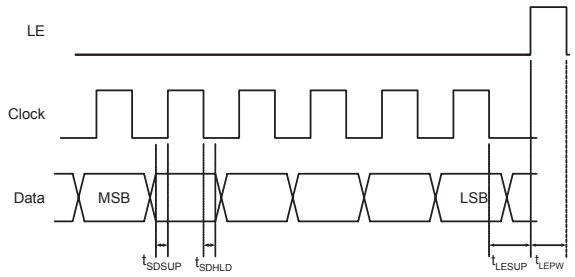


Figure 2. Serial Interface Timing Diagram

Table 3. Serial Interface AC Characteristics

Symbol	Parameter	Min.	Max.	Units
f_{clk}	Serial data clock frequency (Note 1)		10	MHz
t_{clkH}	Serial clock HIGH time	30		ns
t_{clkL}	Serial clock LOW time	30		ns
t_{LESUP}	LE set-up time after last clock falling edge	10		ns
t_{LEPW}	LE minimum pulse width	30		ns
t_{SDSUP}	Serial data set-up time before clock rising edge	10		ns
t_{SDHLD}	Serial data hold time after clock falling edge	10		ns

Note 1. fclk verified during the functional pattern test. Serial programming sections of the functional pattern are clocked at 10MHz to verify fclk specification.

The DVGA3-122+, uses a common 6-bit serial, as shown in Table 4: 6-Bit attenuator Serial Programming Register Map. The first bit, the MSB, corresponds to the 16-dB Step and the last bit, the LSB, corresponds to the 0.5dB step.

Table 4. 6-Bit attenuator Serial Programming Register Map

B5	B4	B3	B2	B1	B0
C16	C8	C4	C2	C1	C0.5

MSB (first in)

LSB (last in)

Power-up Control Settings

The DVGA3-122+ always assumes a specifiable attenuation setting on power-up, allowing a known attenuation state to be established before an initial serial control word is provided. When the attenuator powers up, the six control bits are set to whatever data is present on the six control inputs (C0.5 to C16). This allows any one of the 64 attenuation settings to be specified as the power-up state.

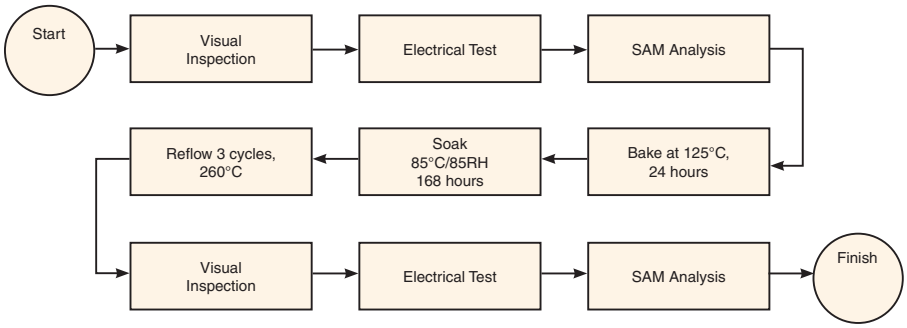
Additional Detailed Technical Information *additional information is available on our dash board. To access this information click here*	
Performance Data	Data Table
	Swept Graphs
	S-Parameter (S2P Files) Data Set (.zip file)
Case Style	DG1677-2 *Plastic package, exposed paddle, lead finish: Matte-Tin*
Tape & Reel **Standard quantities available on reel**	F68 *7" reels with 20,50,100,200, 500 or 1K devices* *13" reels with 2K, 3K, & 4K devices*
Suggested Layout for PCB Design	PL-655
Evaluation Board	TB-DVGA3-122+
Environmental Ratings	ENV08T1

ESD Rating

Human Body Model (HBM): Class 1A (250 to <500V) in accordance with ANSI/ESD STM 5.1 - 2001

MSL Rating

Moisture Sensitivity: MSL1 in accordance with IPC/JEDEC J-STD-020D



Additional Notes

A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.

B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.

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