

Solid state

# USB/I<sup>2</sup>C/SPI SPDT Switch

## U2C-1SP2T-63VH

50Ω 10 to 6000 MHz

### The Big Deal

- USB and I<sup>2</sup>C and SPI power & control
- High power handling (2W, hot switching)
- Ultra high isolation (110 dB over full frequency range)
- Small case (3.0" x 2.0" x 0.47")



Software Package

Generic photo used for illustration purposes only

Case Style: NR2563

Model No.	Description	Qty.
U2C-1SP2T-63VH	Single pole double throw RF Switch	1

#### Included Accessories

MUSB-CBL-3+	3.3 ft USB cable	1
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#### RoHS Compliant

See our web site for RoHS Compliance methodologies and qualifications

### Typical Applications

- Cellular BTS / handset testing
- High volume production testing / ATE
- Design verification testing
- RF signal routing / switch matrices

### Product Overview

Mini-Circuits' U2C-1SP2T-63VH is a high isolation, high power, absorptive SPDT switch with USB, I<sup>2</sup>C and SPI control. The fast switching, solid state switch operates from 10 MHz to 6000 MHz with 700 ns typical transition time. High linearity (+52 dBm typ IP3), and very high isolation (110 dB typical) allow the model to be used for a wide variety of RF applications.

Full software support is provided for USB control, including our user-friendly GUI application for Windows and a full API and programming instructions for both Windows and Linux environments (32-bit and 64-bit systems). The latest version of the full software package can be downloaded from <https://www.minicircuits.com/softwaredownload/solidstate.html> at any time. Alternatively, the SPI and I<sup>2</sup>C interfaces provide options for controlling multiple switches at once via a simple serial interface (typically using a microcontroller), supporting up to 8 switches connected in parallel with I<sup>2</sup>C or up to 30 switches connected in series with SPI.

The U2C-1SP2T-63VH is housed in a compact, rugged metal case (3.0" x 2.0" x 0.47") with 3 SMA (F) connectors (COM, J1 and J2), a USB Mini-B and three 10-pin digital connector for control and power via USB, I<sup>2</sup>C and SPI.

### Key Features

Feature	Advantages
Multiple control interfaces (I <sup>2</sup> C, SPI & USB)	USB provides a quick and easy PC control method with full software support, while I <sup>2</sup> C allows multiple switches to be controlled in parallel from a microcontroller / embedded system using minimal hardware (2 wire control)
RF SPDT absorptive switch	Wideband (10 to 6000 MHz) with low insertion loss (4 dB typ.), high isolation (110 dB typ.), and high power rating (+33 dBm terminated power).
Daisy chain SPI control	Allows connecting up to 30 units in series to a single power supply and SPI control
High Linearity (IP3 +52 dBm typ.)	Results in little or negligible inter-modulation generation, meeting requirements for digital communications signals.
DC Blocking at RF ports	Built in blocking capacitors eliminate the need for external DC blocking circuitry at RF ports.

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Rev. F  
ECO-020129  
EDR-11652  
U2C-1SP2T-63VH  
MCIL  
231212  
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## Electrical Specifications @ 0 to 50°C

Parameter	Port	Conditions	Min.	Typ.	Max.	Units
Operating Frequency			10		6000	MHz
Insertion Loss	COM to any active port	10 to 700 MHz	-	3.2	4.7	dB
		700 to 2500 MHz	-	4.0	5.5	
		2500 to 5000 MHz	-	4.5	6.0	
		5000 to 6000 MHz	-	5.0	6.5	
Isolation	Between ports J1 & J2 (At all states)	10 to 700 MHz	100	105	-	dB
		700 to 2500 MHz	100	110	-	
		2500 to 5000 MHz	100	105	-	
		5000 to 6000 MHz	100	103	-	
	COM to any terminated port (At all states)	10 to 700 MHz	100	110	-	
		700 to 2500 MHz	100	110	-	
		2500 to 5000 MHz	100	110	-	
		5000 to 6000 MHz	100	105	-	
VSWR	COM port in all active states	10 to 700 MHz	-	1.45	-	:1
		700 to 2500 MHz	-	1.30	-	
		2500 to 5000 MHz	-	1.25	-	
		5000 to 6000 MHz	-	1.30	-	
	Any port connected to COM	10 to 700 MHz	-	1.45	-	
		700 to 2500 MHz	-	1.30	-	
		2500 to 5000 MHz	-	1.30	-	
		5000 to 6000 MHz	-	1.30	-	
	Any terminated port <sup>1</sup>	10 to 700 MHz	-	1.30	-	
		700 to 2500 MHz	-	1.30	-	
		2500 to 5000 MHz	-	1.30	-	
		5000 to 6000 MHz	-	1.30	-	
Power Input @ 1 dB Compression <sup>2,3,4</sup>	COM to any active port	100 to 6000 MHz	-	+39.5	-	dBm
IP3 <sup>2,4,5</sup>	COM to any active port	100 to 6000 MHz	-	+52	-	dBm
Transition Time <sup>6</sup>	-	-	-	0.7	2	µs
Minimum dwell time <sup>7</sup>	High Speed Mode	-	-	5	-	µs
Switching Time (USB) <sup>8</sup>	-	-	-	2	-	ms
Supply voltage (Vcc)	USB or I <sup>2</sup> C control	-	4.75	5	5.25	V <sub>DC</sub>
Supply Current (Icc)		-	-	30	50	mA
Operating RF Input Power <sup>3,9</sup>	-	10 to 600 MHz	Max power derates linearly from +33 dBm @ 600 MHz to +19 dBm @ 10 MHz			dBm
		600 to 6000 MHz	-	-	+33	

<sup>1</sup> VSWR of COM port In disconnected state is the same as of other terminated ports.

<sup>2</sup> Do not exceed absolute maximum ratings in table on page 3

<sup>3</sup> The model can handle Max RF input from both J1 and J2 at once. Max power derates linearly from +33 dBm @ 600 MHz to +19 dBm @ 10 MHz

<sup>4</sup> Compression and IP3 may degrade below 100 MHz

<sup>5</sup> IP3 tested with 1 MHz span between signals, +5 dBm per tone.

<sup>6</sup> Transition time spec represents the time that the RF signal paths are interrupted during switching and thus is specified without communication delays.

<sup>7</sup> Minimum dwell time is the shortest time that can be achieved between 2 switch transitions when programming an automated switch sequence.

<sup>8</sup> Switching time(USB) is the time from issuing a single software command via USB to the switch state changing. The most significant factor is the host PC, influenced by CPU load and USB protocol. The time shown is an estimate for a medium CPU load and USB 2.0 connection.

<sup>9</sup> At high power input additional cooling may be needed.

## DC Electrical Specifications for SPI Control

Parameter	Min.	Typ.	Max.	Units
Vcc, Supply Voltage	12	—	24	V <sub>DC</sub>
Load on Vcc between In and Out ports	—	0.05	—	Ω
Icc, Supply Current	@24V	—	15	mA
	@12V	—	30	
Control Current	—	400	—	µA

## Control voltages for SPI & I<sup>2</sup>C Control

Parameter	Min.	Typ.	Max.	Units
Control Input Low	SPI	-0.3	—	+0.6
	I <sup>2</sup> C	0	—	0.8
Control Input High	SPI	2.0	—	5.5
	I <sup>2</sup> C	2.0	—	3.3

## Absolute Maximum Ratings

Operating Temperature		0°C to 50°C
Storage Temperature		-20°C to 60°C
Max Case Temperature		80°C
DC supply voltage max.	@ USB port (USB or I <sup>2</sup> C control)	6V
	@ I <sup>2</sup> C pin 10 (USB or I <sup>2</sup> C control)	6V
	@ SPI In / Out pins 1-3 (for SPI control)	26V
Voltage on I <sup>2</sup> C control pins (Pins 7 & 8)		3.6V
Voltage on SPI control pins (Pins 7-9)		6V
Voltage on address pins (4 - 6 in I <sup>2</sup> C )		3.6V
RF power @ 10 - 600 MHz into any RF port		Derate linearly from +34 dBm @ 600 MHz to +20 dBm @ 10 MHz
RF power @ 600 - 6000 MHz into any RF port		+34 dBm
DC voltage @ RF Ports		12V

Permanent damage may occur if any of these limits are exceeded. Operating in the range between operating power limits and absolute maximum ratings for extended periods of time may result in reduced life and reliability.

## Connections

RF Switch (J1 to J4, COM)	(SMA female)
USB	(USB type Mini-B receptacle)
I <sup>2</sup> C*	(10 pin Hirose DF11 socket) <sup>8</sup>
SPI In*	(10 pin Hirose DF11 socket) <sup>8</sup>
SPI Out*	(10 pin Hirose DF11 socket) <sup>8</sup>

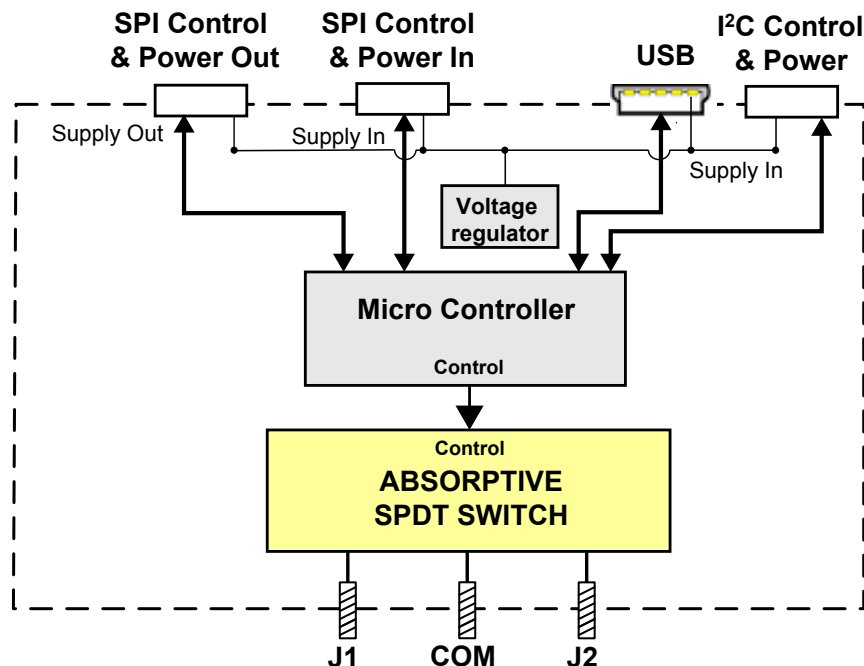
<sup>8</sup> Mating connector is Hirose DF11-10DS-2C(20)

## \*Pin Connections for all Hirose DF11 connectors

Pin Number	I <sup>2</sup> C connector	SPI In	SPI Out
1	GND	Supply voltage (Vcc)	Supply voltage (Vcc)
2	GND	Supply voltage (Vcc)	Supply voltage (Vcc)
3	GND	Supply voltage (Vcc)	Supply voltage (Vcc)
4	A0	GND	GND
5	A1	GND	GND
6	A2	GND	GND
7	SDA	Data In	Data Out
8	SCL	Clock In	Clock Out
9	GND	LE In	LE Out
10	Supply voltage (Vcc)	Blank in	Blank Out

## Block Diagram

**Note:** Power supply is needed from only one port at a time. Power can be supplied to USB port, I<sup>2</sup>C port, or SPI in port according to the control method used. 'SPI Control & Power Out' port is used only to transfer power and control to additional units when connecting multiple units in "Daisy Chain" configuration.



## SPI Control Interface

The U2C-1SP2T-63VH SPI serial interface consists of 2 control bits per unit that select the desired switch state, as shown in Table 1: Switch Logic Table.

Switch state	A0	A1	Port behavior		
			COM	J1	J2
Disconnected	0	0	Terminated Internally (50Ω)	Terminated Internally (50Ω)	Terminated Internally (50Ω)
COM -> 1	1	0	Connected to J1	Connected to COM	Terminated Internally (50Ω)
COM -> 2	0	1	Connected to J2	Terminated Internally (50Ω)	Connected to COM

The serial interface is a 8-bit serial in, parallel-out shift register buffered by a transparent latch. It is controlled by three-wire SPI protocol using Data, Clock and Latch Enable (LE), with an additional Blanking input. All signal voltages are compatible with TTL and LVTTTL. The serial input and output ports allow up to 30 switches to be connected in a “Daisy Chain” configuration, with SPI data being passed down the chain from Master to Slaves.

## Blank Input

- Allows the SPI control input to be turned on and off to prevent spurious / inadvertent data entry
- When Blank is high, the SPI interface works as below using the data, clock and LE inputs.
- When Blank is low, the SPI interface is disabled so the data, clock and LE inputs have no effect, and all SPI Out pins are kept at digital low, regardless of input.
- It is recommended to hold Blank low when the switch will be operating in a given state for long periods, and only bring it to high when loading data in the shift register to set the switch state.

## Data & Clock Inputs

- 8 data bits must be loaded for switch control but only the last 2 bits (LSB) are used to define the switch state (refer to table 1 above)
- Where multiple switches are connected in a daisy-chain configuration, 8 bits must be loaded per switch:
  - ◊ The first 8 bits loaded define the state for the final switch in the chain
  - ◊ The final 8 bits loaded are applied to the first switch in the chain

## Latch Enable(LE) Input

- When LE is high, the latch is transparent and the switch state will change as data is clocked into the shift register
- When LE is low, data can be clocked into the shift register without affecting the switch state.
- The recommended process is to hold LE low while clocking in data, then toggle LE high and low again to latch the switch state
- If multiple switches are connected in daisy-chain setup, the data for all switches in the chain should be loaded before toggling LE high and low.

## Note:

1. In Daisy Chain setup, LE will be connected in parallel to all units using the switches’ internal buffers to prevent control current from increasing as more units are connected.
2. In Daisy Chain setup, Blank will be connected directly to all units, causing the control current to increase as the more units are connected.

SPI Control Interface(Continued)

Blank	LE	Digital control status	
		Shift register	Latch
0	0	Parallel Output Locked	Locked
1	0	Active	Locked
0	1	Parallel Output Locked	Locked
1	1	Parallel Output Locked	Transparent

Figure 1: Serial Interface Timing Diagram

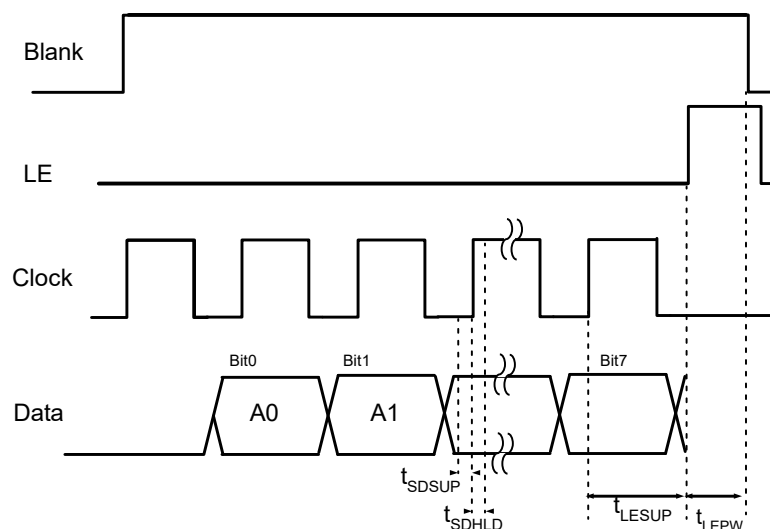


Table 2. Serial Interface AC Characteristics

Symbol	Parameter	Min.	Max.	Units
$f_{clk}$	Serial data clock frequency		20	MHz
$t_{clkH}$	Serial clock HIGH time	8		ns
$t_{clkL}$	Serial clock LOW time	14		ns
$t_{LESUP}$	LE set-up time after last clock rising edge	8		ns
$t_{LEPW}$	LE minimum pulse width	8		ns
$t_{SDSUP}$	Serial data set-up time before clock rising edge	8		ns
$t_{SDHLD}$	Serial data hold time after clock falling edge	1		ns

SPI Control Interface (Daisy Chain)

Figure 2: Connection diagram for multiple units in series

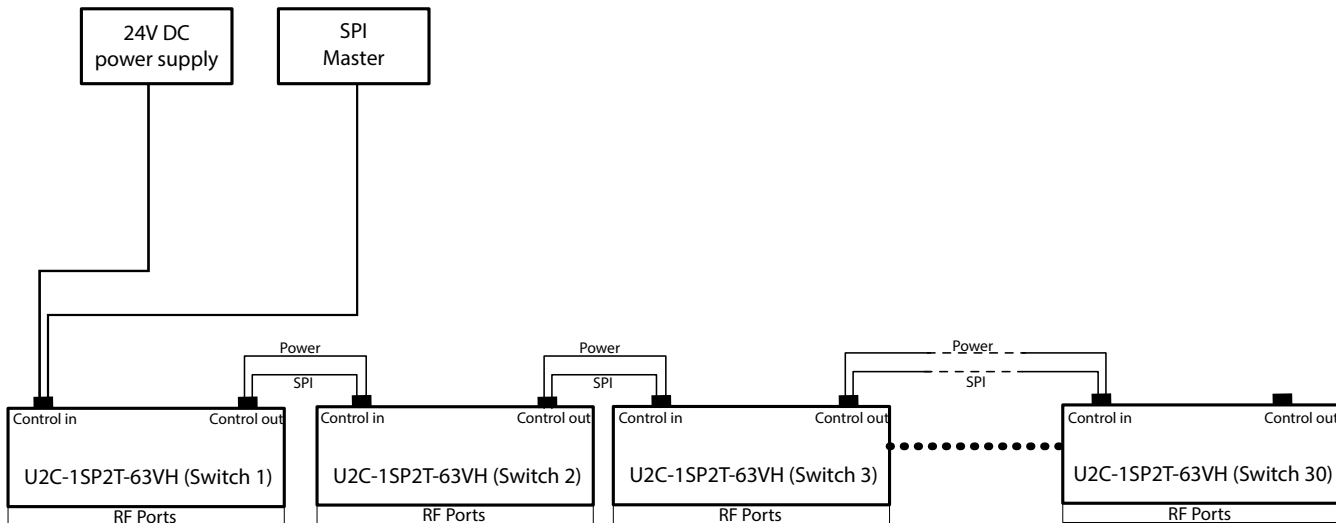


Figure 3: SPI Timing Diagram for 3 units in series

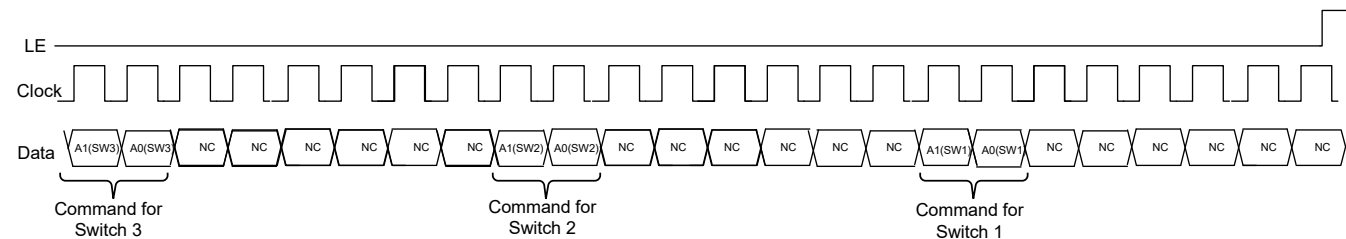
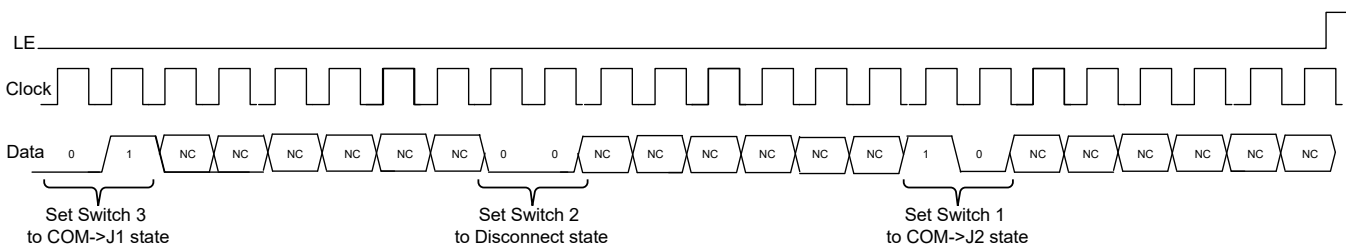
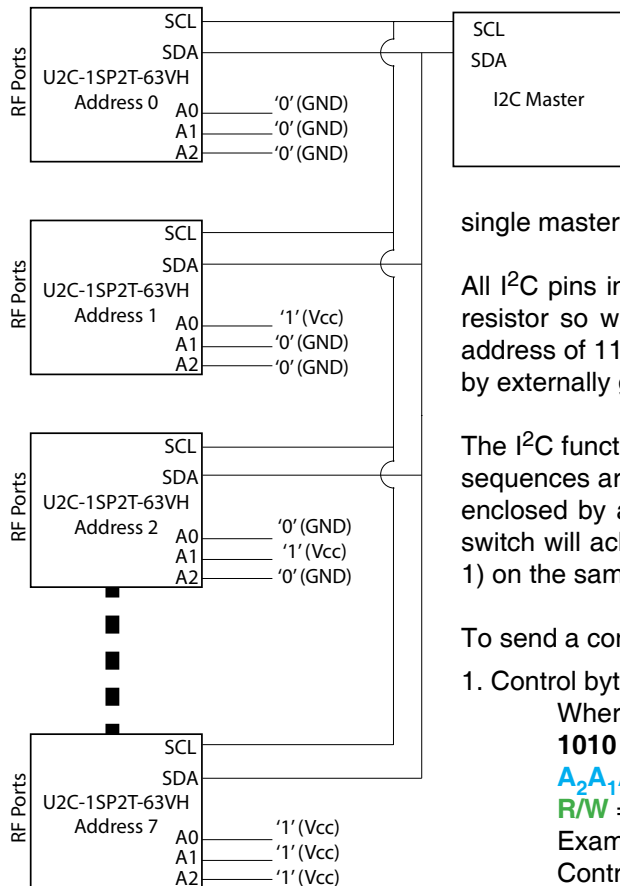


Figure 4: Example of command for 3 switches in series



I<sup>2</sup>C communication parameters

Parameter	Conditions		Min.	Typ.	Max.	Units
Voltage levels	Logic High Voltage	Input	2.0	-	3.3	V
	Logic Low Voltage	Input	0	-	0.8	
Clock Frequency	-		-	-	400	kHz



The I<sup>2</sup>C is a short-range synchronous communication protocol for simple 2-wire communication with slave devices using clock (SCL) and data (SDA) connections. The U2C-1SP2T-63VH interface also includes 3 address pins (A0, A1 and A2), allowing up to 8 switches to be controlled independently from a single master with shared SDA and SCL connections.

All I<sup>2</sup>C pins in the U2C-1SP2T-63VH are connected to an internal pullup resistor so will float to logic 1 when disconnected. This sets a default address of 111 for all units (decimal 7). Addresses from 0 to 7 can be set by externally grounding the relevant address pins (A0, A1 and A2).

The I<sup>2</sup>C functionality is limited to setting or reading switch states. Control sequences are sent to the switch in several bytes on the data connection, enclosed by a start and stop signal, and clocked at up to 400 kHz. The switch will acknowledge each byte received with a single “ACK” bit (logic 1) on the same data connection.

To send a command to the switch 3 bytes will be sent:

1. Control byte (1010A<sub>2</sub>A<sub>1</sub>A<sub>0</sub>R/W)

Where:

**1010** = Control code for U2C-1SP2T-63VH

**A<sub>2</sub>A<sub>1</sub>A<sub>0</sub>** = 3-bit address for the U2C-1SP2T-63VH switch module

**R/W** = Read / write select bit ('0' to write or '1' to read)

Example:

Control byte = **10101000**

Address = **100** (binary) = 4 (decimal)

R/W = **0** (write to switch)

2. Switch selector byte (00000001) - U2C-1SP2T-63VH contains only 1 switch so this byte is always 00000001.
3. Switch state byte (00000XYZ) - The switch state, represented by a binary string according to the truth table below.

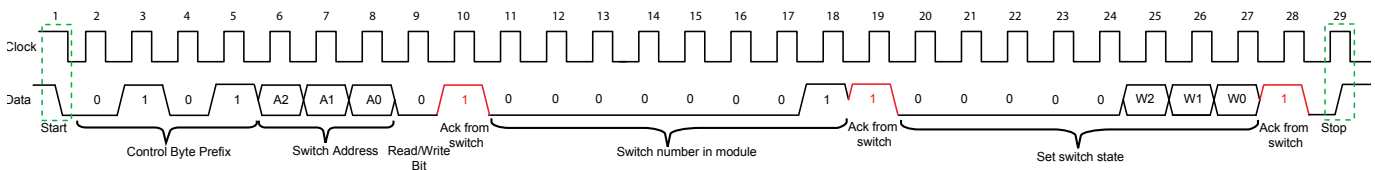
Switch state	Switch state byte	Port behavior		
		COM	J1	J2
Disconnected	0000 0000	Terminated Internally (50Ω)	Terminated Internally (50Ω)	Terminated Internally (50Ω)
COM -> 1	0000 0001	<b>Connected to J1</b>	<b>Connected to COM</b>	Terminated Internally (50Ω)
COM -> 2	0000 0010	<b>Connected to J2</b>	Terminated Internally (50Ω)	<b>Connected to COM</b>

In I<sup>2</sup>C protocol the Data line may not change states while the Clock is high, except for the start and stop signals which enclose each sequence of bytes. While the Clock is high a falling edge (transition from logic 1 to logic 0) signifies the start of a sequence, while a rising edge (transition from logic 0 to logic 1) signifies a stop signal. All other transitions must occur while the clock is low.

## Setting switch state via I<sup>2</sup>C

The I<sup>2</sup>C communication sequence to set the switch state is:

1. Start signal
2. Send control byte (write mode)
3. Receive ACK response from switch
4. Send switch selector byte
5. Receive ACK response from switch
6. Send switch state byte
7. Receive ACK response from switch
8. Stop signal



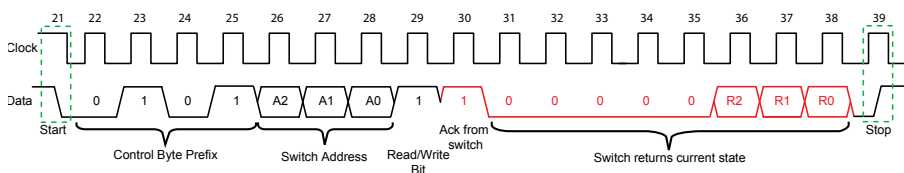
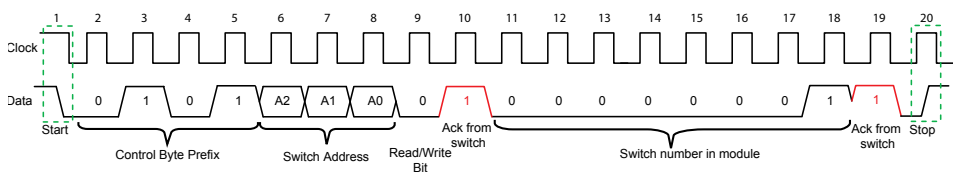
### Legend:

Signal from master to switch —————  
 Signal from switch to master —————

## Reading switch state via I<sup>2</sup>C

The I<sup>2</sup>C communication sequence to set the switch state is:

- |                                     |                                     |
|-------------------------------------|-------------------------------------|
| 1. Start signal                     | 7. Start signal                     |
| 2. Send control byte (write mode)   | 8. Send control byte (read mode)    |
| 3. Receive ACK response from switch | 9. Receive ACK response from switch |
| 4. Send switch selector byte        | 10. Receive current switch state    |
| 5. Receive ACK response from switch | 11. Stop signal                     |
| 6. Stop signal                      |                                     |

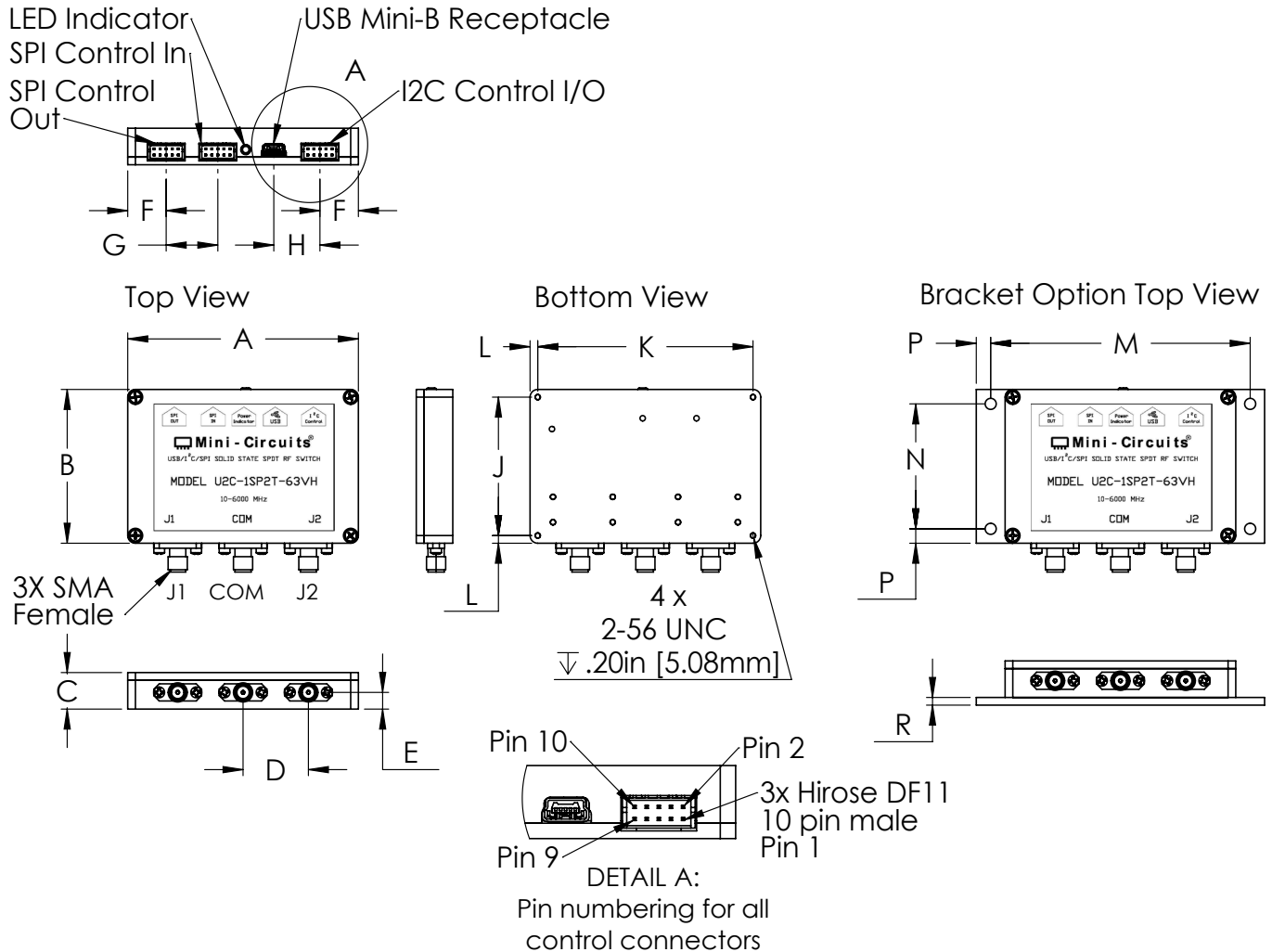


### Legend:

Signal from master to switch —————  
 Signal from switch to master —————



## Outline Drawing (NR2563)



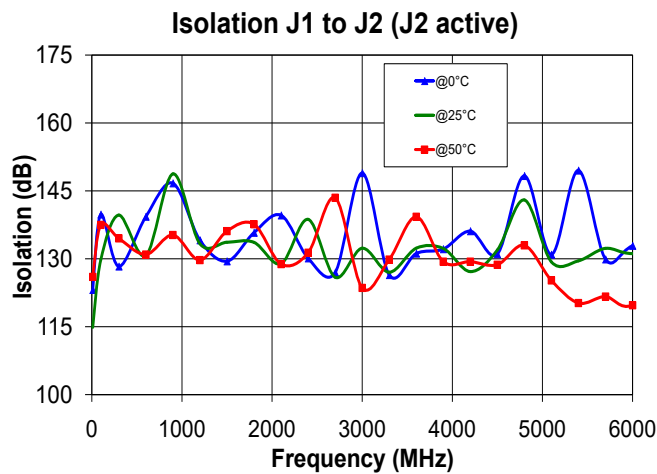
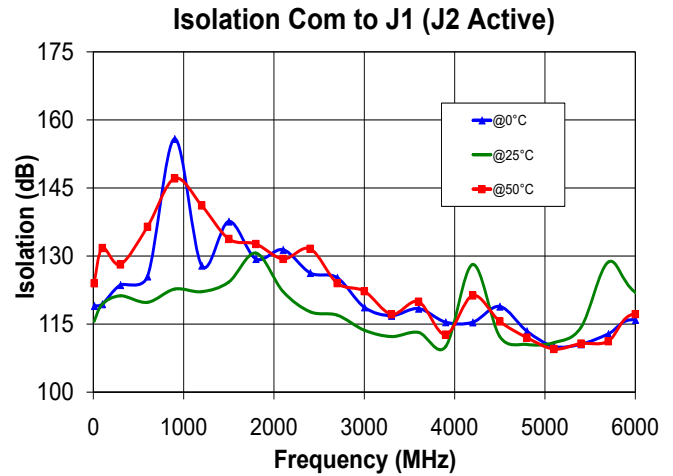
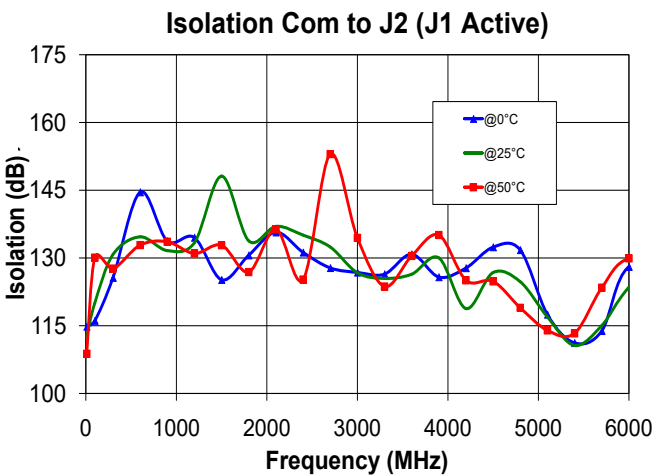
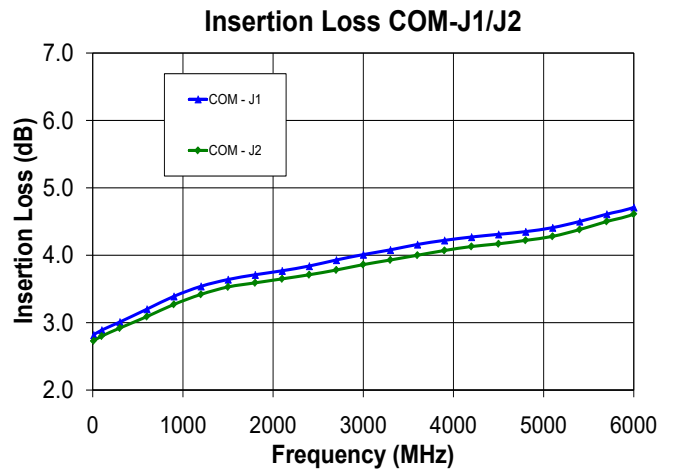
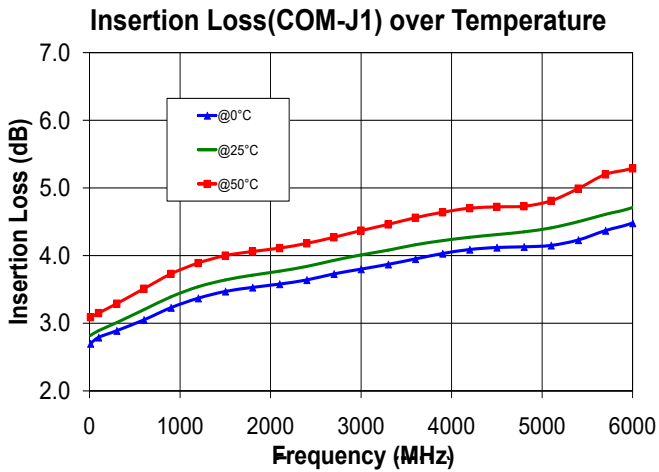
**Case Material** - Aluminum alloy

**Case Finish** - Clear chemical conversion coating, non-chrome or trivalent chrome based

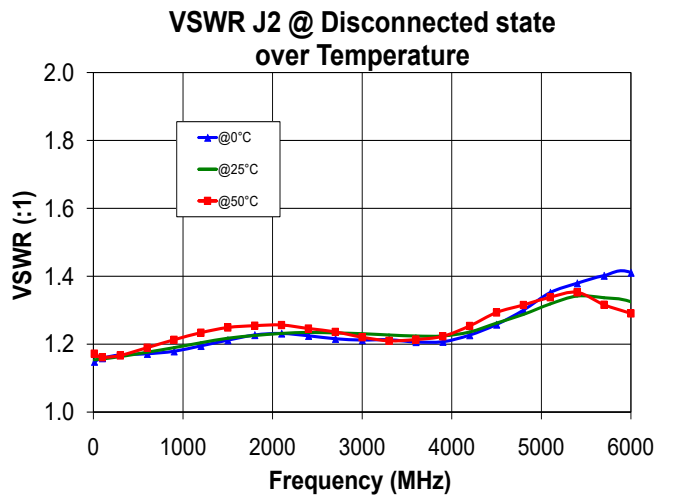
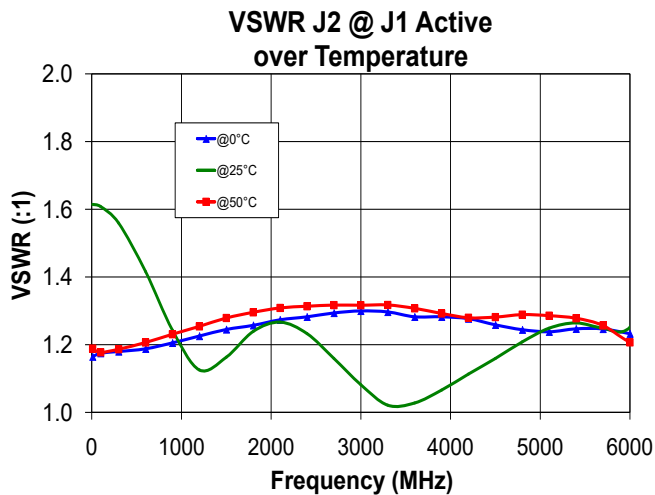
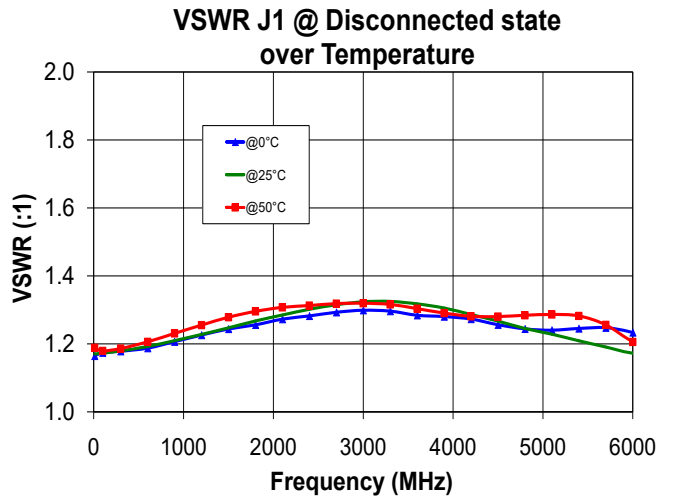
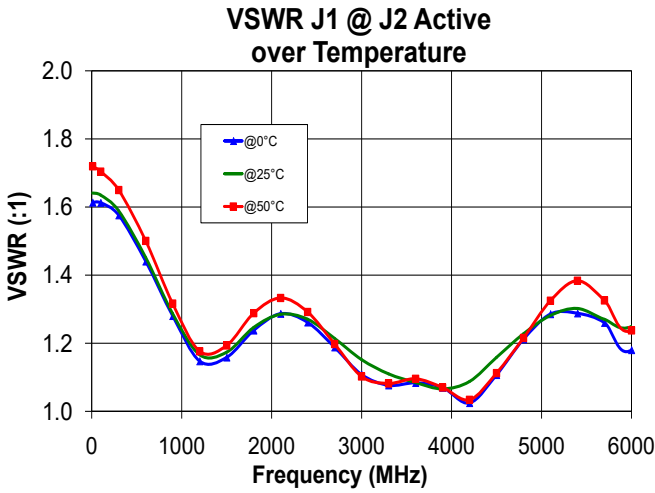
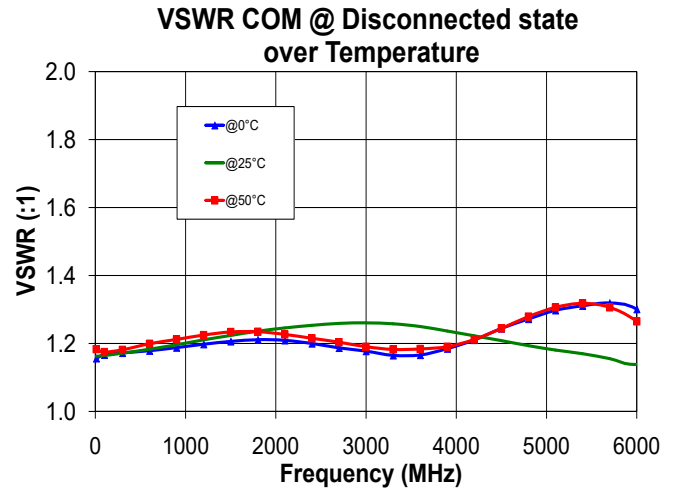
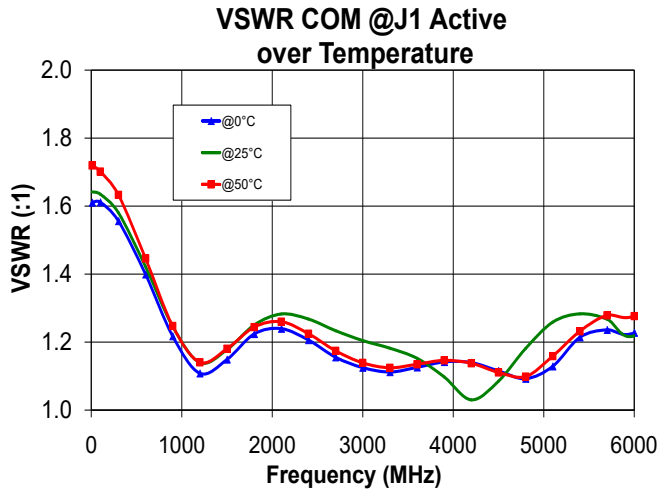
### Outline Dimensions (inch / mm)

A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	WT. GRAMS
3.000	2.000	0.475	0.850	0.217	0.500	0.672	0.600	1.800	2.800	0.100	3.375	1.625	0.188	0.144	0.100	100
76.20	50.80	12.07	21.59	5.51	12.70	17.07	15.24	45.72	71.12	2.54	85.73	41.28	4.77	3.66	2.54	

Typical Performance Curves



Typical Performance Curves (Continued)



## Software & Documentation Download:

- Mini-Circuits' full software and support package including user guide, Windows GUI, DLL files, programming manual and examples can be downloaded free of charge from <https://www.minicircuits.com/softwaredownload/solidstate.html>
- Please contact [testsolutions@minicircuits.com](mailto:testsolutions@minicircuits.com) for support

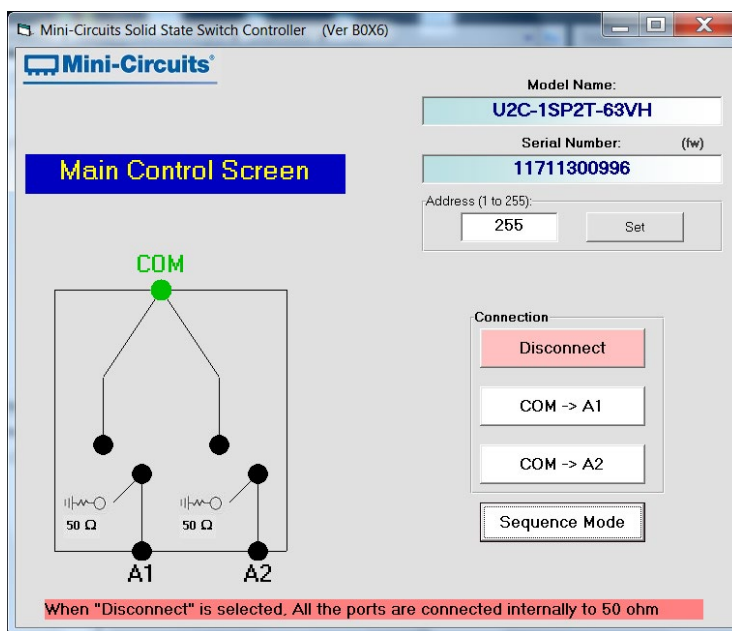
## Minimum System Requirements

Parameter	Requirements	
Interface	USB HID or I <sup>2</sup> C	
System requirements	GUI:	Windows 7 or later
	USB API (ActiveX & .Net)	Windows 7 or later and programming environment with ActiveX or .Net support
	I <sup>2</sup> C or SPI	Any computer with a suitable I/O port
	USB direct programming support	Linux, Windows 7 or later
Hardware	Intel i3 (or equivalent) or later	

## Graphical User Interface (GUI) for Windows

### Key Features:

- Set switch manually
- Set timed sequence of switching states
- Configure switch address and upgrade Firmware



## Application Programming Interface (API)

### Windows Support:

- API DLL files exposing the full switch functionality
  - ActiveX COM DLL file for creation of 32-bit programs
  - .Net library DLL file for creation of 32 / 64-bit programs
- Supported by most common programming environments (refer to application note [AN-49-001](#) for summary of tested environments)

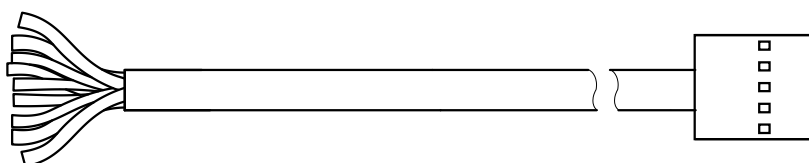
### Linux Support:

- Full switch control in a Linux environment is achieved by way of USB interrupt commands.

## Recommended Accessories

An optional cable accessory for SPI and I<sup>2</sup>C control which is available with U2C-1SP2T-63VH, the CBL-DF11-3FPD+ 'pig tail' cable. CBL-DF11-3FPD+ is a shielded cable with a 'pig tail' (bare wires) end allowing customer to assemble their own cable with any connector they need. Cable length is 4.9 feet / 1.5 meters using 32 AWG wires.


**Control Cable CBL-DF11-3FPD+**



Pin Number	when used for SPI control		when used for I <sup>2</sup> C control		Pigtail Wire Color
	Function	Description	Function	Description	
1	Vcc	Supply Voltage	GND	Ground connection	WHITE
2	Vcc	Supply Voltage	GND	Ground connection	BLACK
3	Vcc	Supply Voltage	GND	Ground connection	RED
4	GND	Ground connection	A0	Set Address bit A0	GREEN
5	GND	Ground connection	A1	Set Address bit A1	YELLOW
6	GND	Ground connection	A2	Set Address bit A2	BLUE
7	Data	Data for SPI	SDA	Data for I <sup>2</sup> C	BROWN
8	Clock	Clock for SPI	SCL	Clock for I <sup>2</sup> C	ORANGE
9	LE	Latch Enable for SPI	GND	Ground connection	GRAY
10	Blank	Blank for SPI	Vcc	Supply Voltage	VIOLET

Ordering, Pricing & Availability Information see our web site

Model	Description
U2C-1SP2T-63VH	USB & I <sup>2</sup> C Single Pole double Throw Switch

Included Accessories	Part No.	Description
	MUSB-CBL-3+	3.3 ft (1.0 m) USB Cable: USB type A(Male) to USB type Mini-B(Male)

Optional Accessories	Part No.	Description
	MUSB-CBL-3+ (Spare)	3.3 ft (1.0 m) USB Cable: USB type A(Male) to USB type Mini-B(Male)
	MUSB-CBL-7+	6.6 ft (2.0 m) USB Cable: USB type A(Male) to USB type Mini-B(Male)
See Previous page	CBL-DF11-3FPD+	3 ft (0.9 m) I <sup>2</sup> C & SPI Cable: DF11(plug) to Pigtail 32 AWG wires
	USB-AC/DC-5+	AC/DC +5V power adaptor with USB connector <sup>9,10</sup>
See outline drawing	BKT-39-23+	Bracket kit including 3.75" x 2.00" bracket, mounting screws and washers

<sup>9</sup> The USB-AC/DC-5 may be used to provide additional power if needing to connect a number of switches in series exceeding 500mA total current draw.

<sup>10</sup> Includes power plugs for US, UK, EU, IL, AU & China. Plugs for other countries are also available, if you need a power plug for a country not listed please contact [testsolutions@minicircuits.com](mailto:testsolutions@minicircuits.com)

## Additional Notes

- A. Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- B. Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
- C. The parts covered by this specification document are subject to Mini-Circuits standard limited warranty and terms and conditions (collectively, "Standard Terms"); Purchasers of this part are entitled to the rights and benefits contained therein. For a full statement of the Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website at [www.minicircuits.com/MCLStore/terms.jsp](http://www.minicircuits.com/MCLStore/terms.jsp)